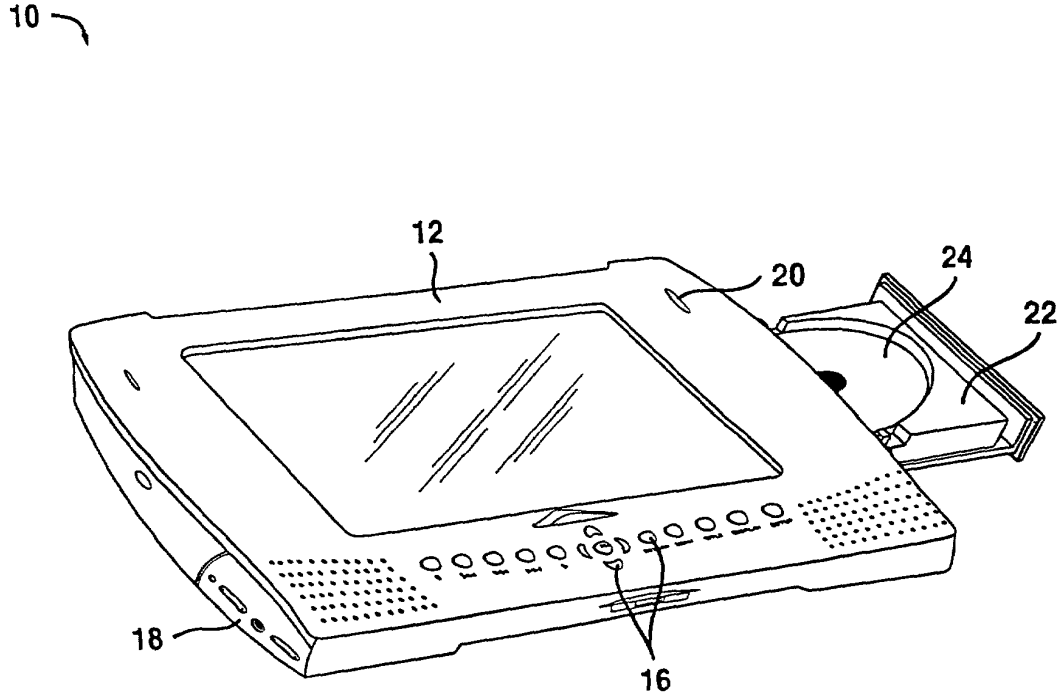

Fig. 1A

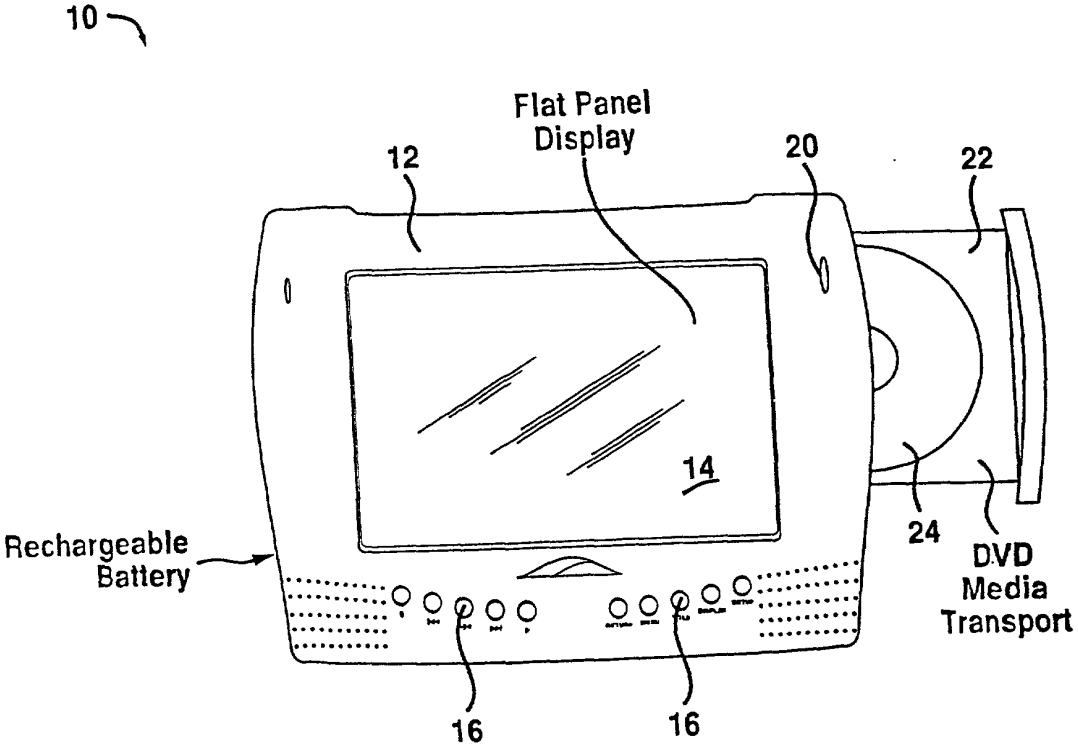
10
Flat Panel Display
12
20
22
14
24
DVD Media Transport
Rechargeable Battery
16
16

Fig. 1B

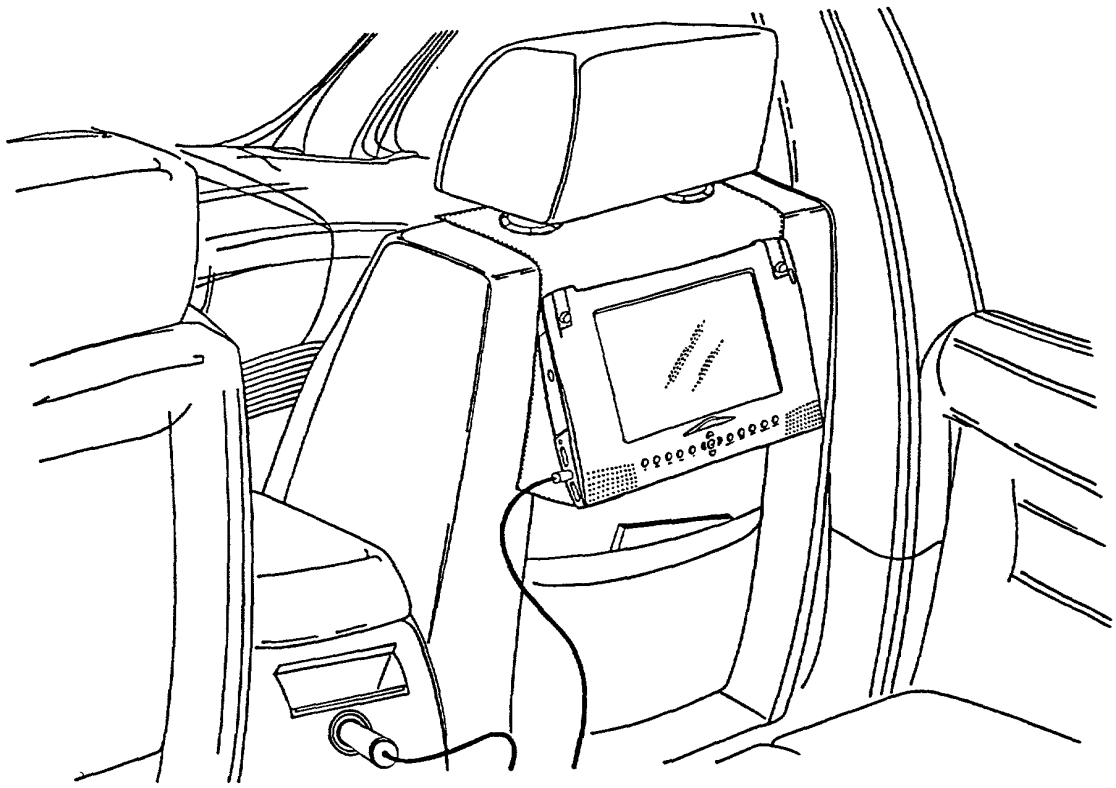

Fig. 2A

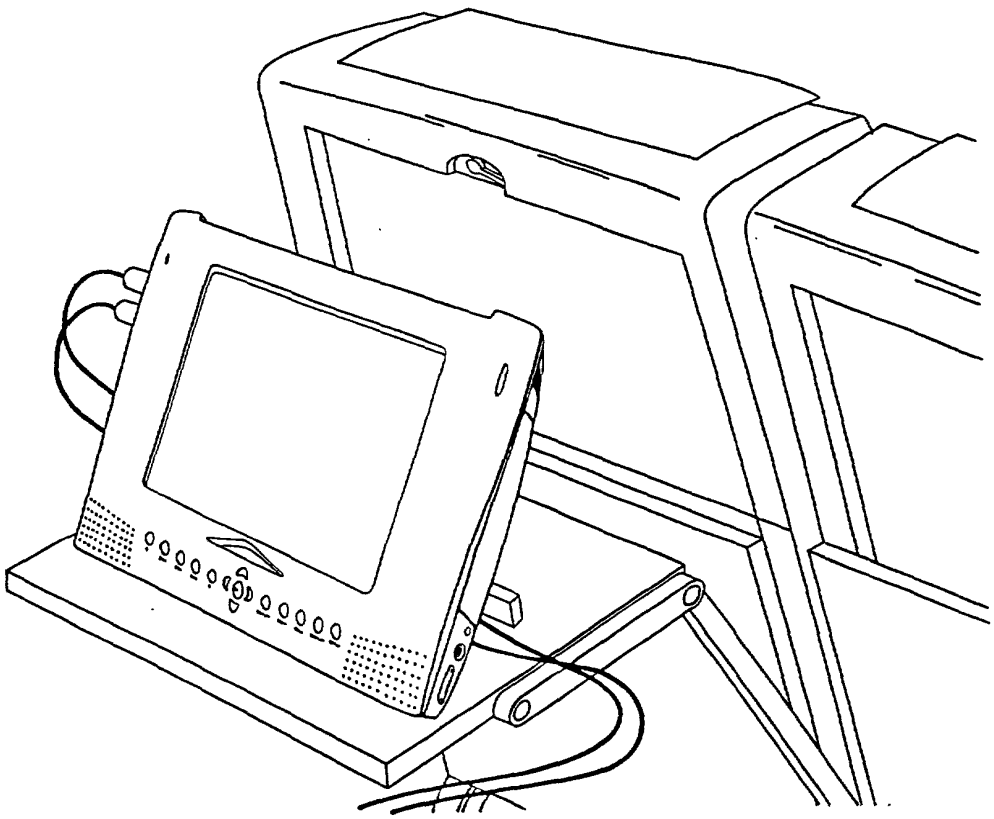

Fig. 2B

Fig. 2C

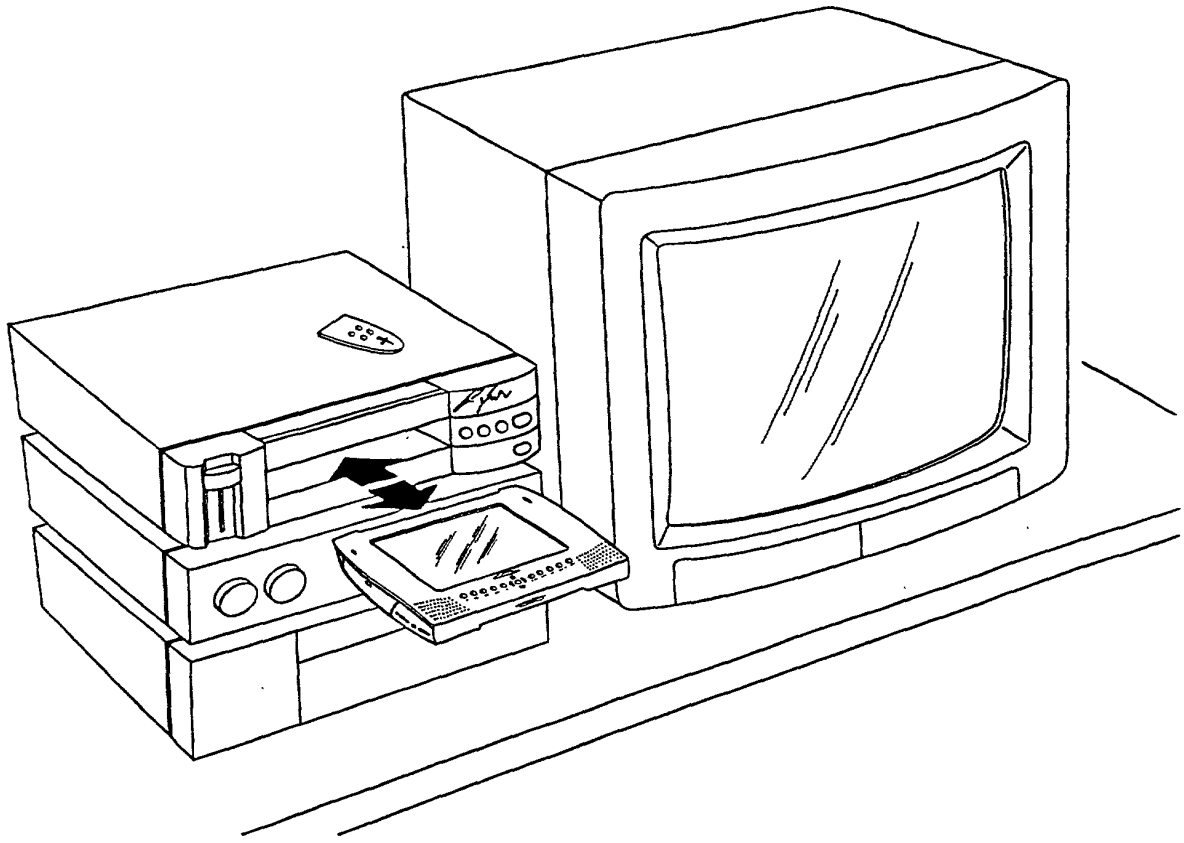

Fig. 2D

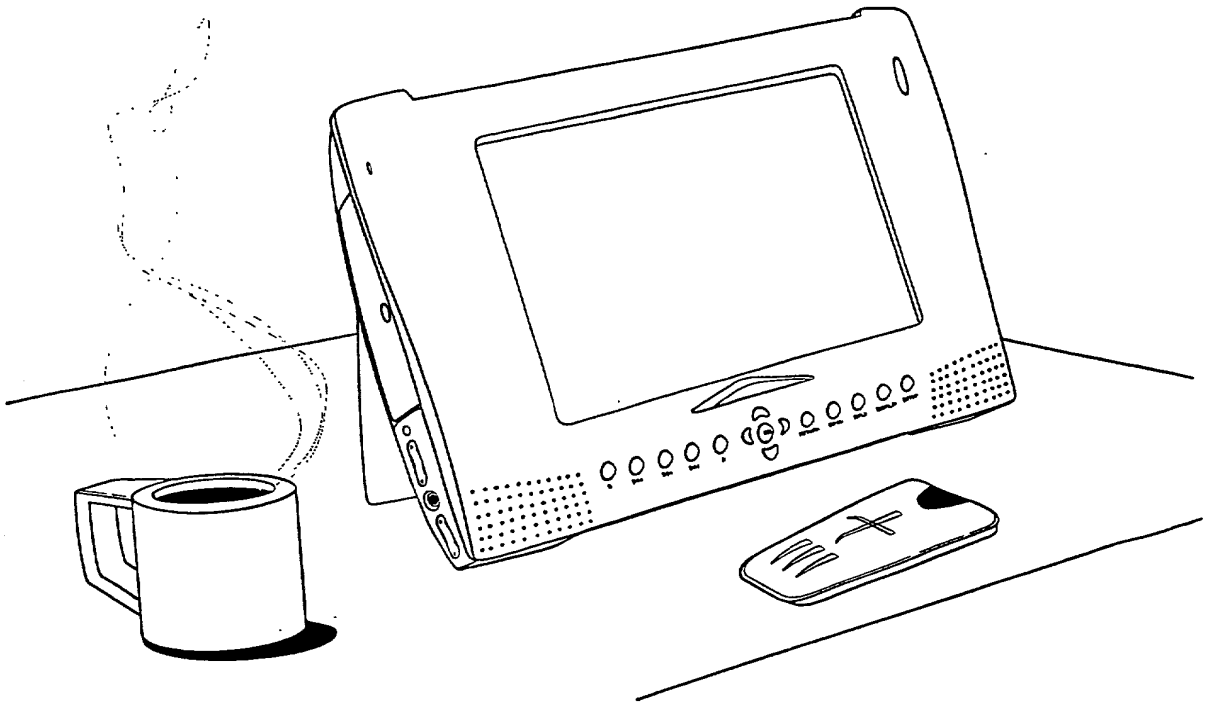

Fig. 2E

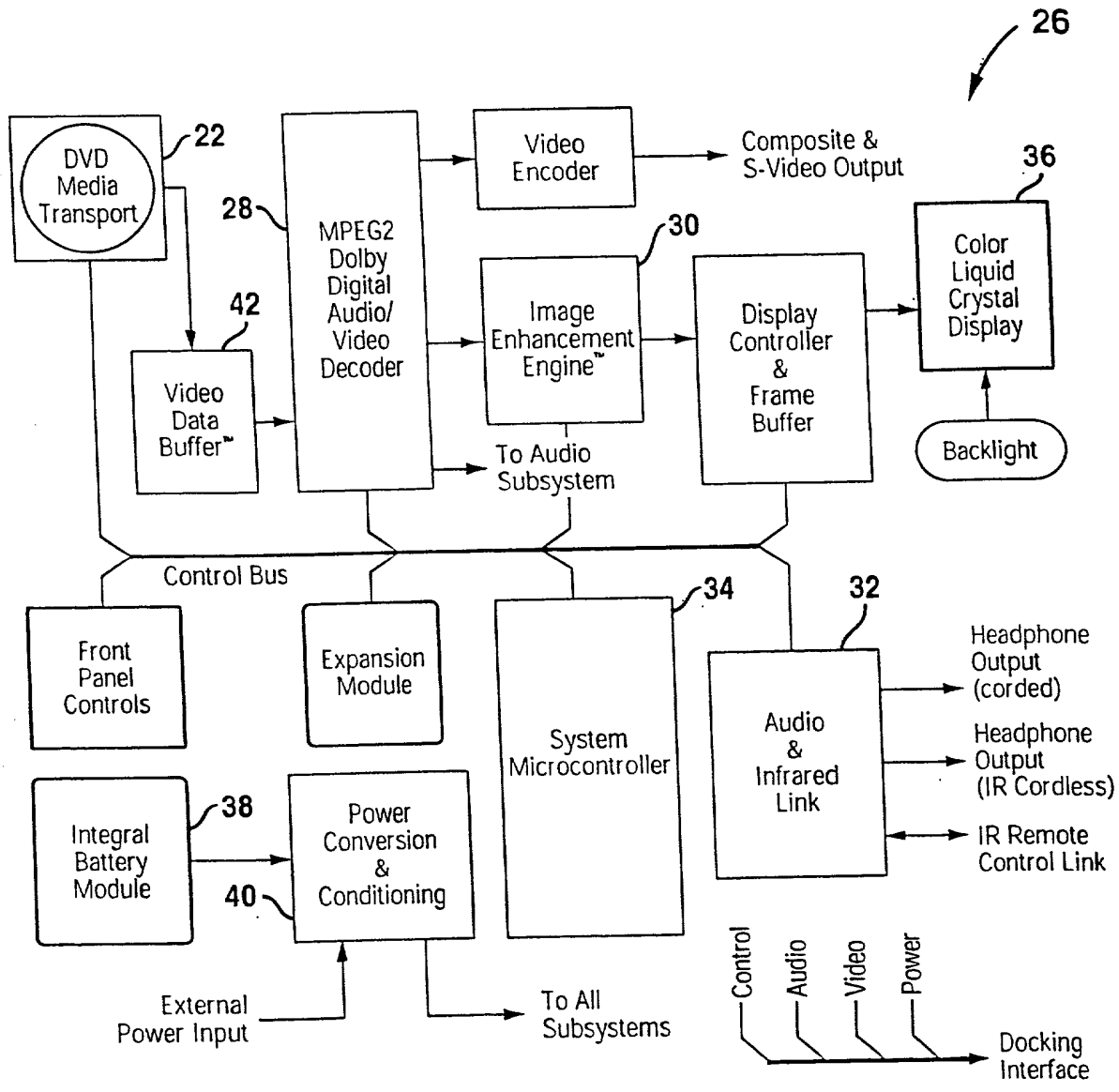
26
DVD Media Transport
22
28
MPEG2 Dolby Digital Audio/ Video Decoder
Video Encoder
Composite & S-Video Output
36
30
Image Enhancement Engine™
Display Controller & Frame Buffer
Color Liquid Crystal Display
42
Video Data Buffer™
To Audio Subsystem
Backlight
Control Bus
Front Panel Controls
Expansion Module
34
System Microcontroller
32
Audio & Infrared Link
Headphone Output (corded)
Headphone Output (IR Cordless)
IR Remote Control Link
38
Integral Battery Module
40
Power Conversion & Conditioning
External Power Input
To All Subsystems
Control
Audio
Video
Power
Docking Interface

Fig. 3

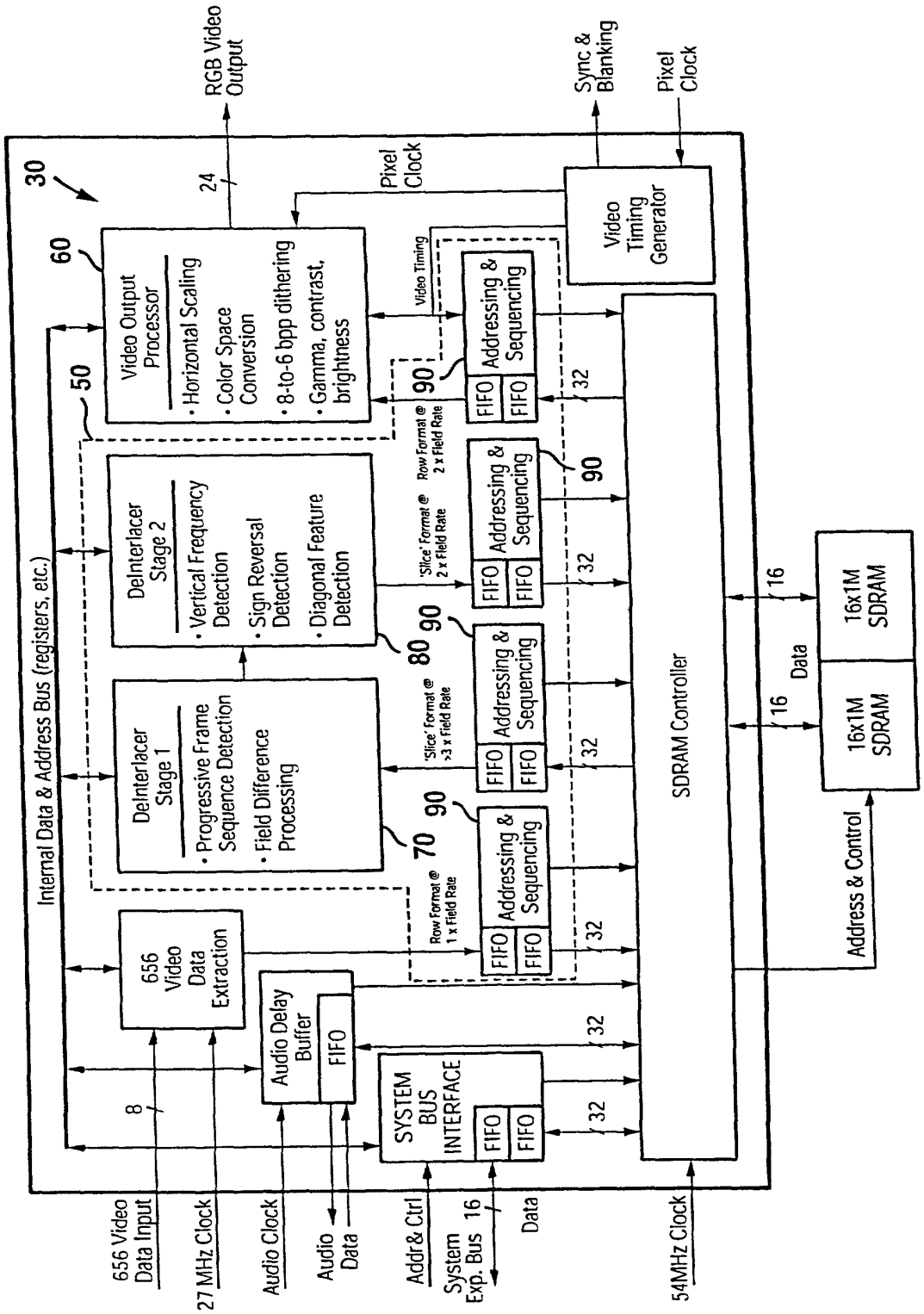
30
Internal Data & Address Bus (registers, etc.)
656 Video Data Input
27 MHz Clock
Audio Clock
Audio Data
Addr & Ctrl
System Exp. Bus
16
Data
54MHz Clock
8
656 Video Data Extraction
Audio Delay Buffer
FIFO
SYSTEM BUS INTERFACE
FIFO
FIFO
32
DeInterlacer Stage 1
• Progressive Frame Sequence Detection
• Field Difference Processing
70
DeInterlacer Stage 2
• Vertical Frequency Detection
• Sign Reversal Detection
• Diagonal Feature Detection
80
50
Video Output Processor
• Horizontal Scaling
• Color Space Conversion
• 8-to-6 bpp dithering
• Gamma, contrast, brightness
60
24
RGB Video Output
Pixel Clock
Sync & Blanking
Video Timing Generator
Video Timing
90
Addressing & Sequencing
FIFO
FIFO
'Slice' Format @ ~3 x Field Rate
Row Format @ 1 x Field Rate
'Slice' Format @ 2 x Field Rate
Row Format @ 2 x Field Rate
SDRAM Controller
Address & Control
16
Data
16x1M SDRAM
16x1M SDRAM

Fig. 4

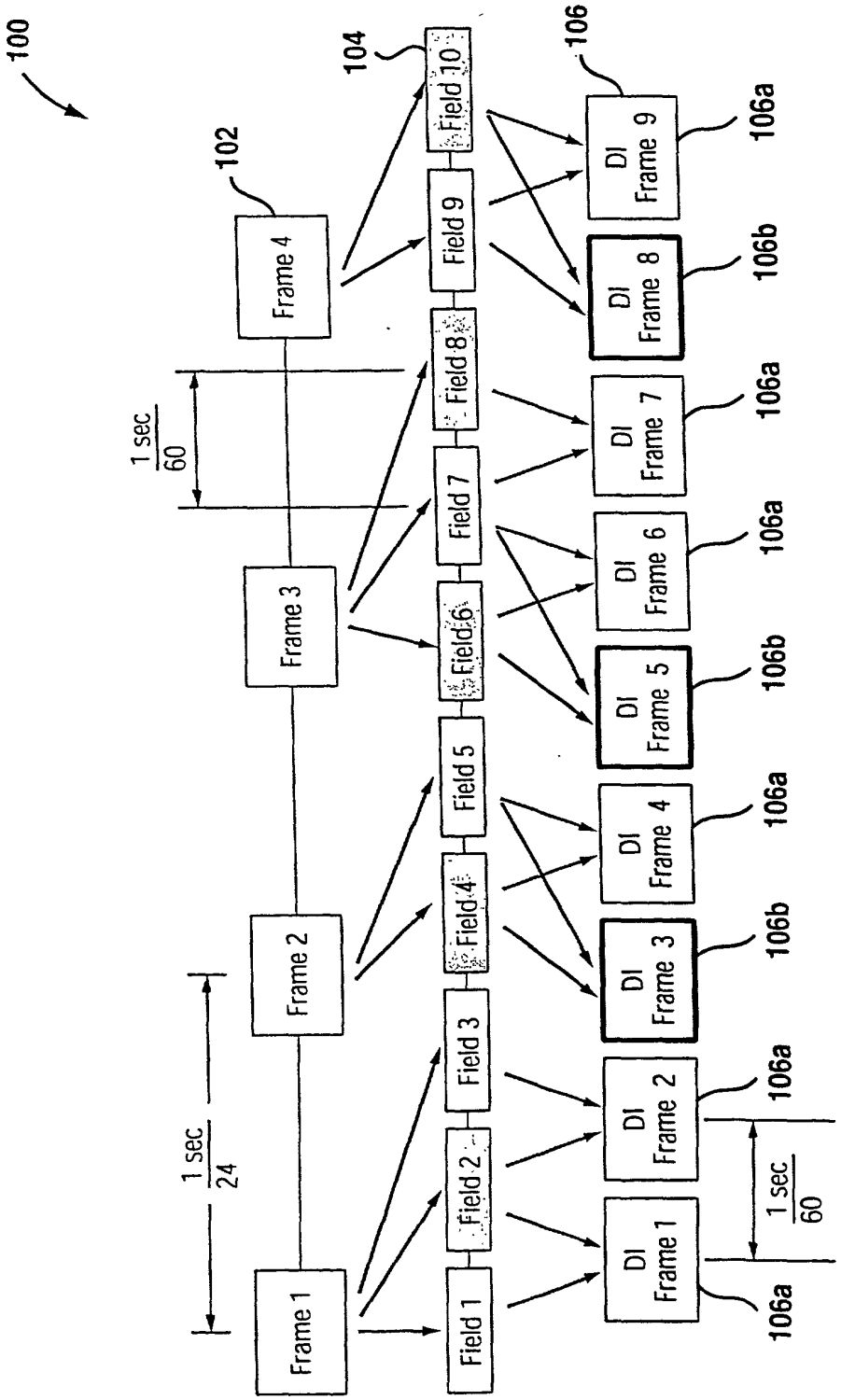
100
102
104
106
Frame 1
Frame 2
Frame 3
Frame 4
Field 1
Field 2
Field 3
Field 4
Field 5
Field 6
Field 7
Field 8
Field 9
Field 10
DI Frame 1
DI Frame 2
DI Frame 3
DI Frame 4
DI Frame 5
DI Frame 6
DI Frame 7
DI Frame 8
DI Frame 9
1 sec / 24
1 sec / 60
1 sec / 60
106a
106b

Fig. 5

20TTh0" 9ET2E00T

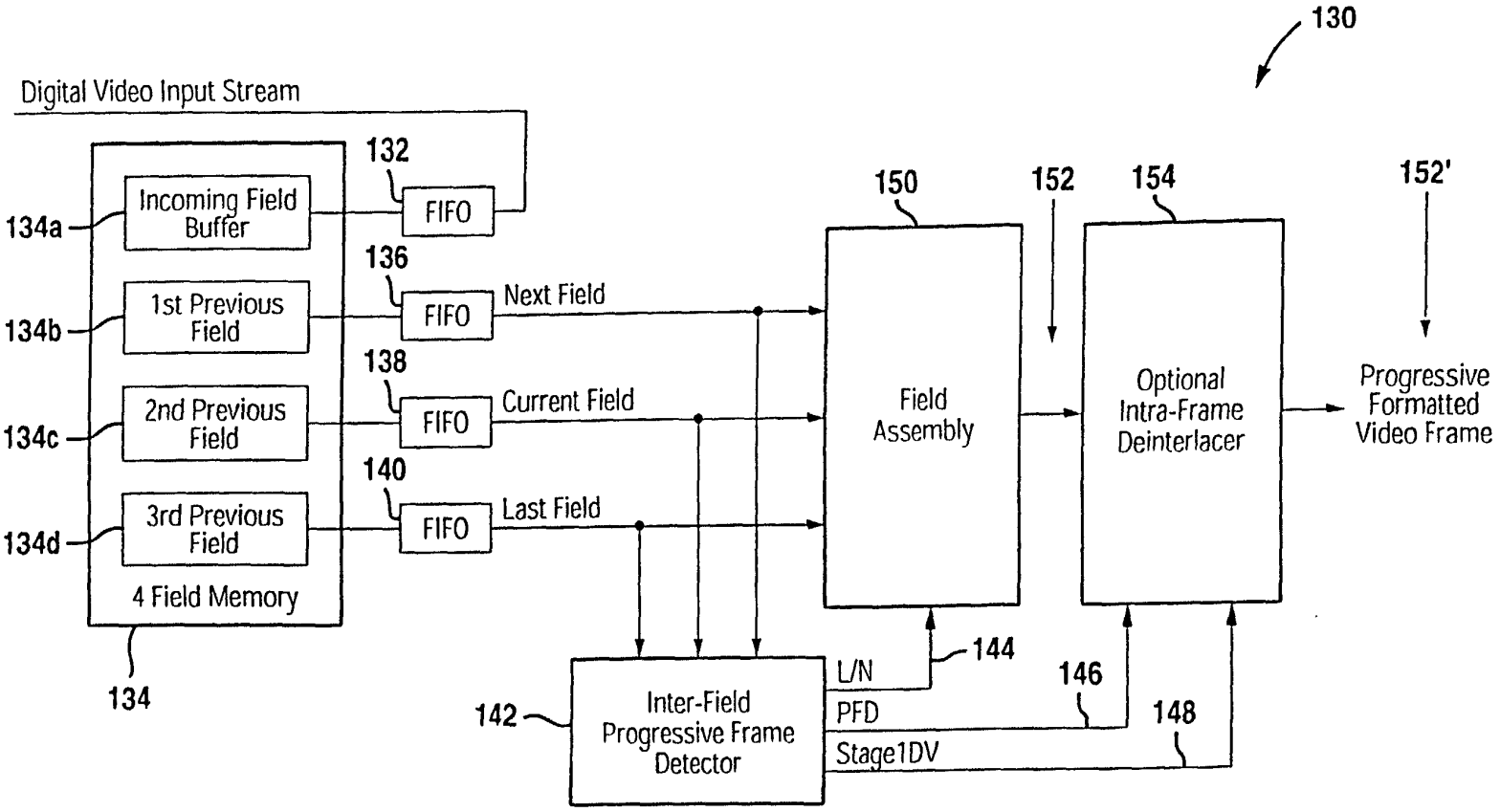

Fig. 6

OPPENHEIMER WOLFF & DONNELLY, LLP
Title: DIGITAL VIDEO SYSTEM AND METYHODS FOR PROVIDING SAME
U.S. Patent Application No. 10/032,136
Atty. Docket No.: 60472-301302
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20Tho" 9ET2E00T

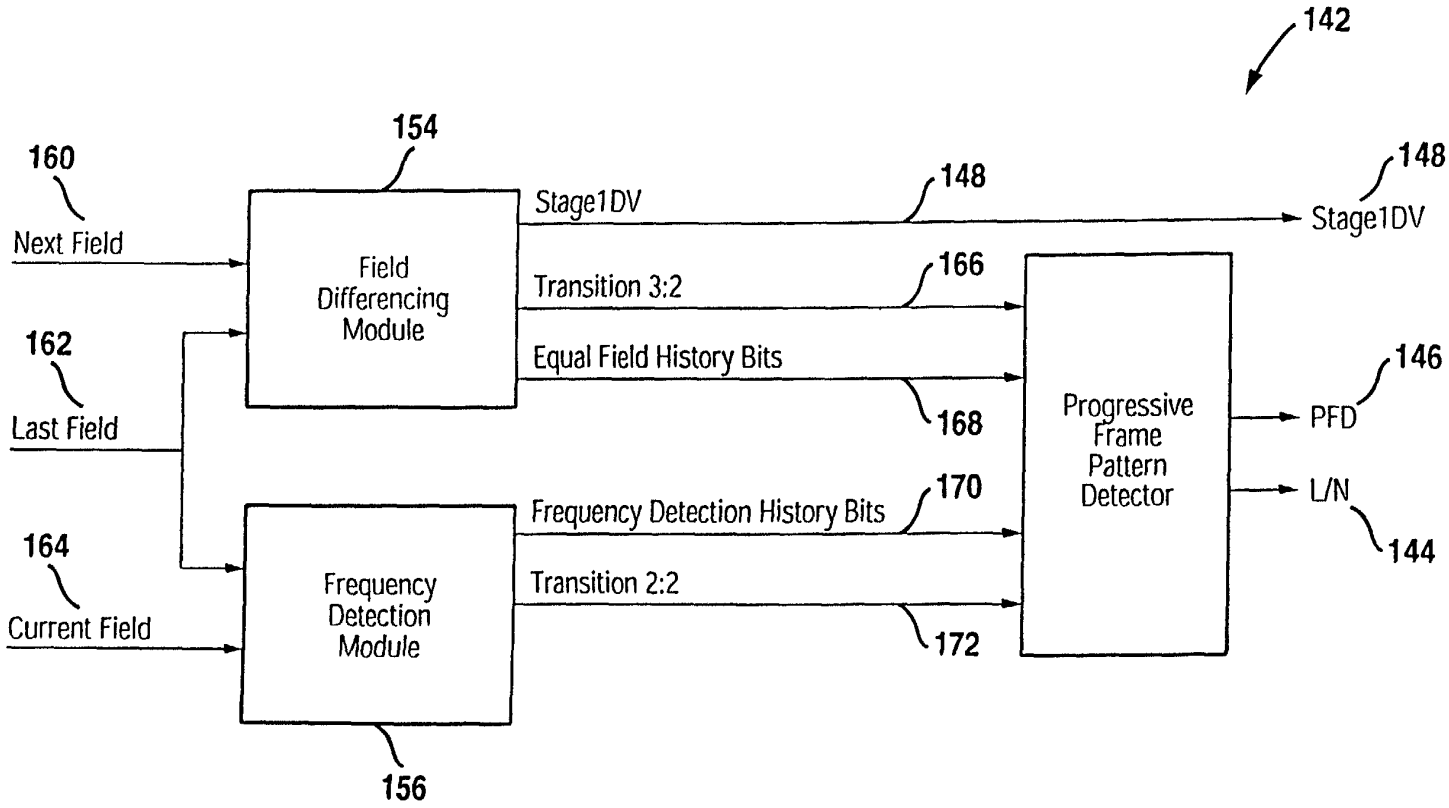

Fig. 7

OPPENHEIMER WOLFF & DONNELLY, LLP
Title: DIGITAL VIDEO SYSTEM AND METYHODS FOR PROVIDING SAME
U.S. Patent Application No. 10/032,136
Atty. Docket No.: 60472-301302
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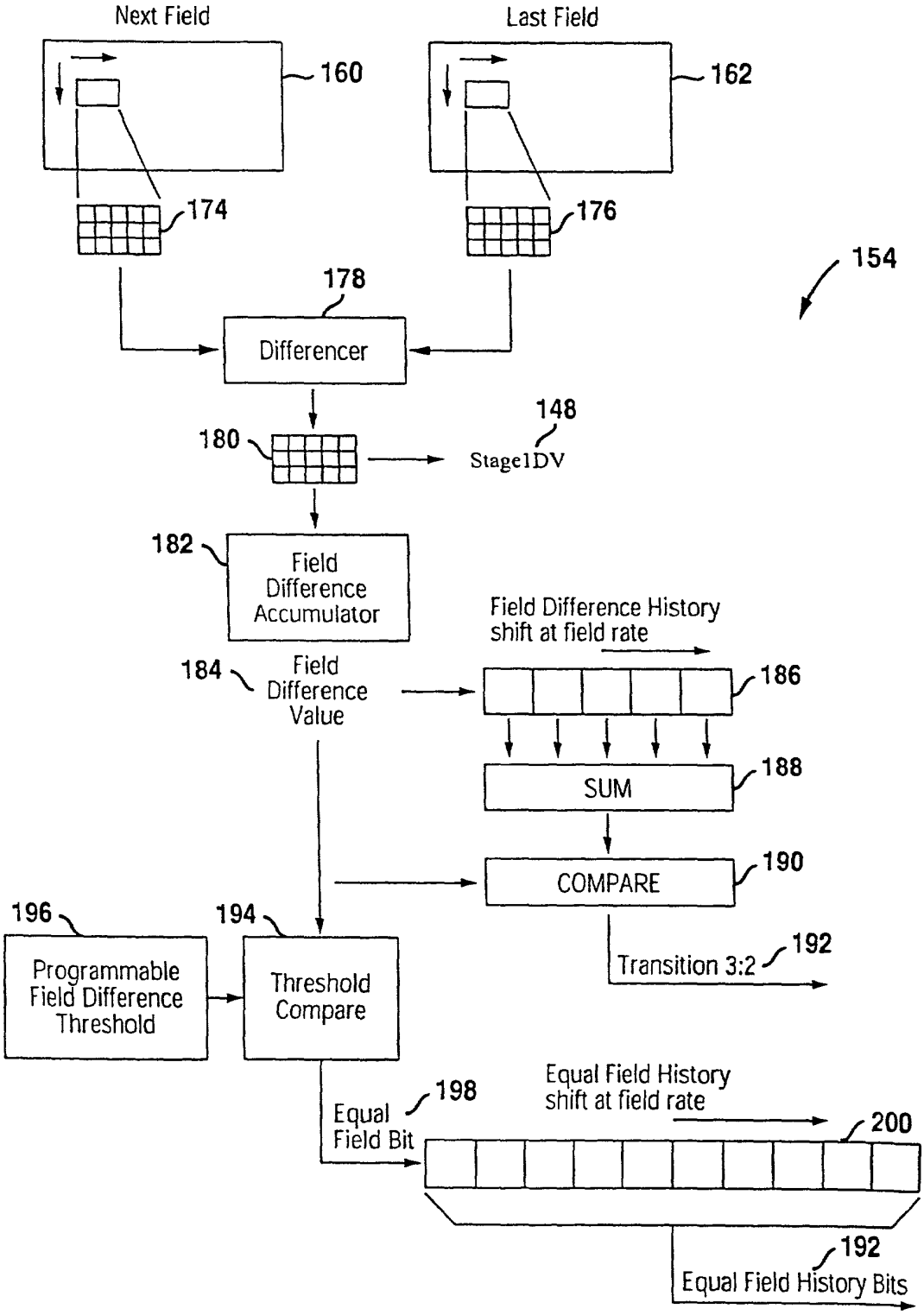

Fig. 8

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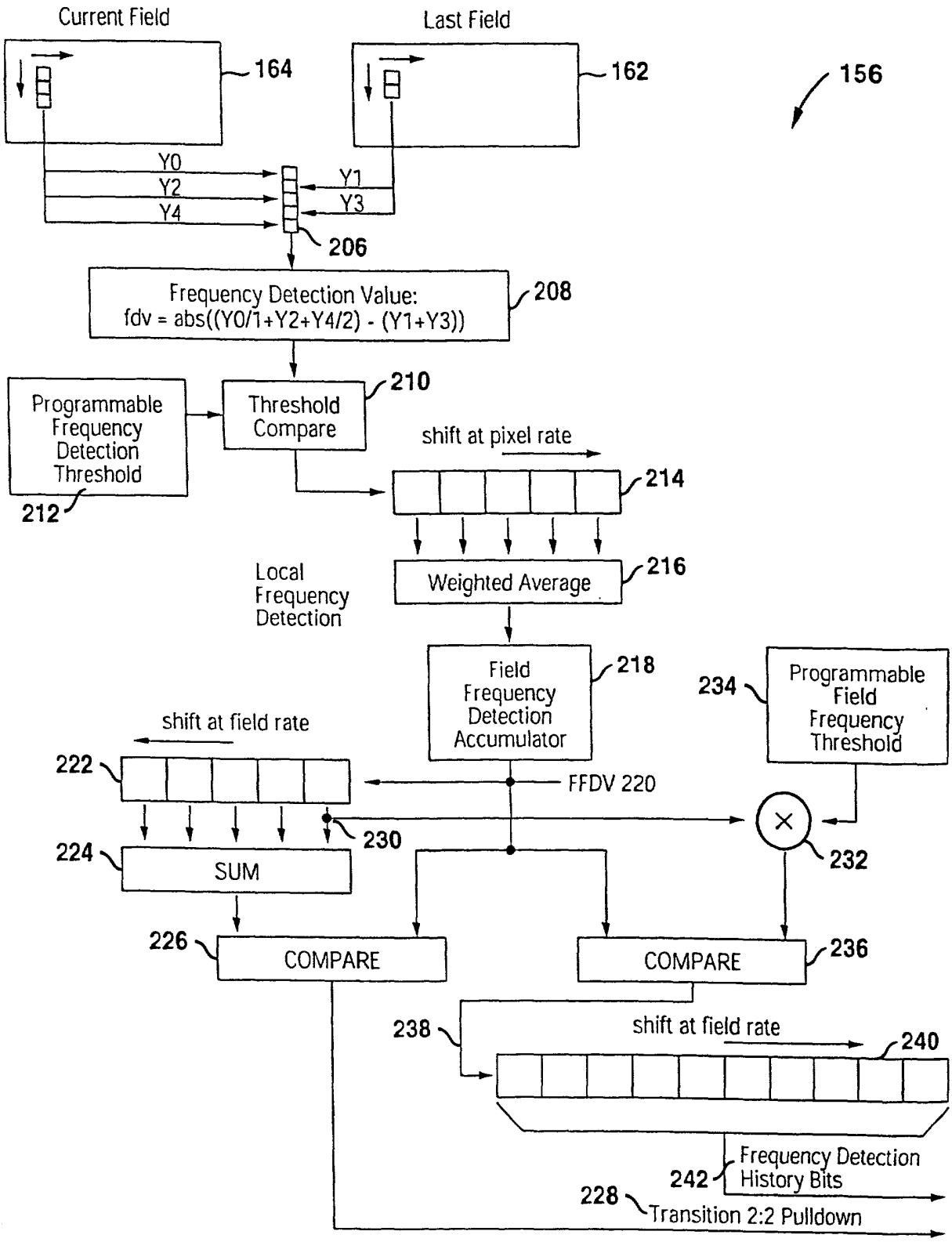
Current Field
Last Field
164
162
156
Y0
Y2
Y4
Y1
Y3
206
Frequency Detection Value:
fdv = abs((Y0/1+Y2+Y4/2) - (Y1+Y3))
208
Programmable Frequency Detection Threshold
212
Threshold Compare
210
shift at pixel rate
214
Local Frequency Detection
Weighted Average
216
Field Frequency Detection Accumulator
218
234
Programmable Field Frequency Threshold
shift at field rate
222
FFDV 220
230
224
SUM
232
226
COMPARE
COMPARE
236
238
shift at field rate
240
Frequency Detection History Bits
242
228
Transition 2:2 Pulldown

Fig. 9

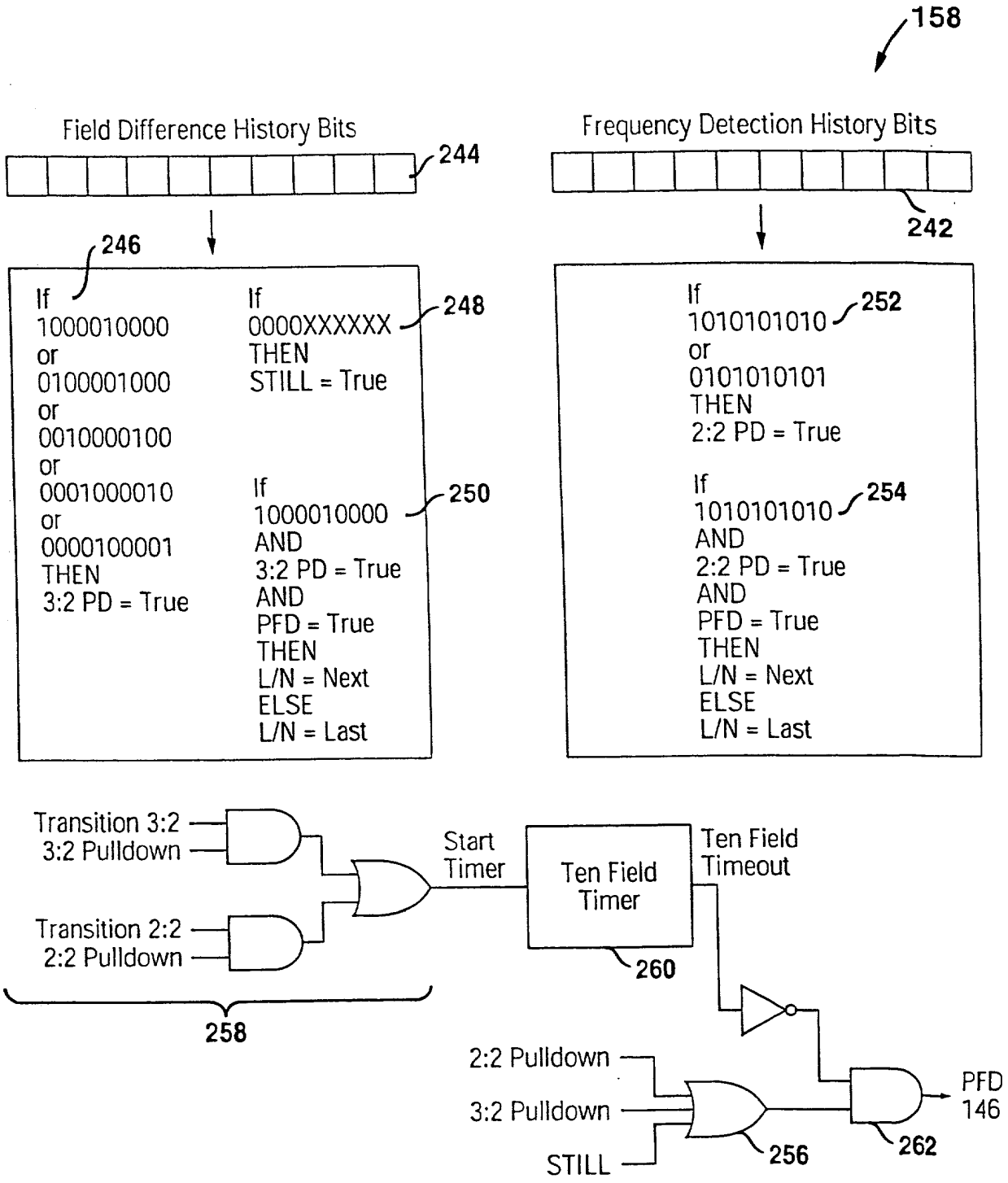
158
Field Difference History Bits
244
246
If
1000010000
or
0100001000
or
0010000100
or
0001000010
or
0000100001
THEN
3:2 PD = True
If
0000XXXXXX
THEN
STILL = True
248
If
1000010000
AND
3:2 PD = True
AND
PFD = True
THEN
L/N = Next
ELSE
L/N = Last
250
Frequency Detection History Bits
242
If
1010101010
or
0101010101
THEN
2:2 PD = True
252
If
1010101010
AND
2:2 PD = True
AND
PFD = True
THEN
L/N = Next
ELSE
L/N = Last
254
Transition 3:2
3:2 Pulldown
Transition 2:2
2:2 Pulldown
258
Start
Timer
Ten Field
Timer
260
Ten Field
Timeout
2:2 Pulldown
3:2 Pulldown
STILL
256
262
PFD
146

Fig. 10

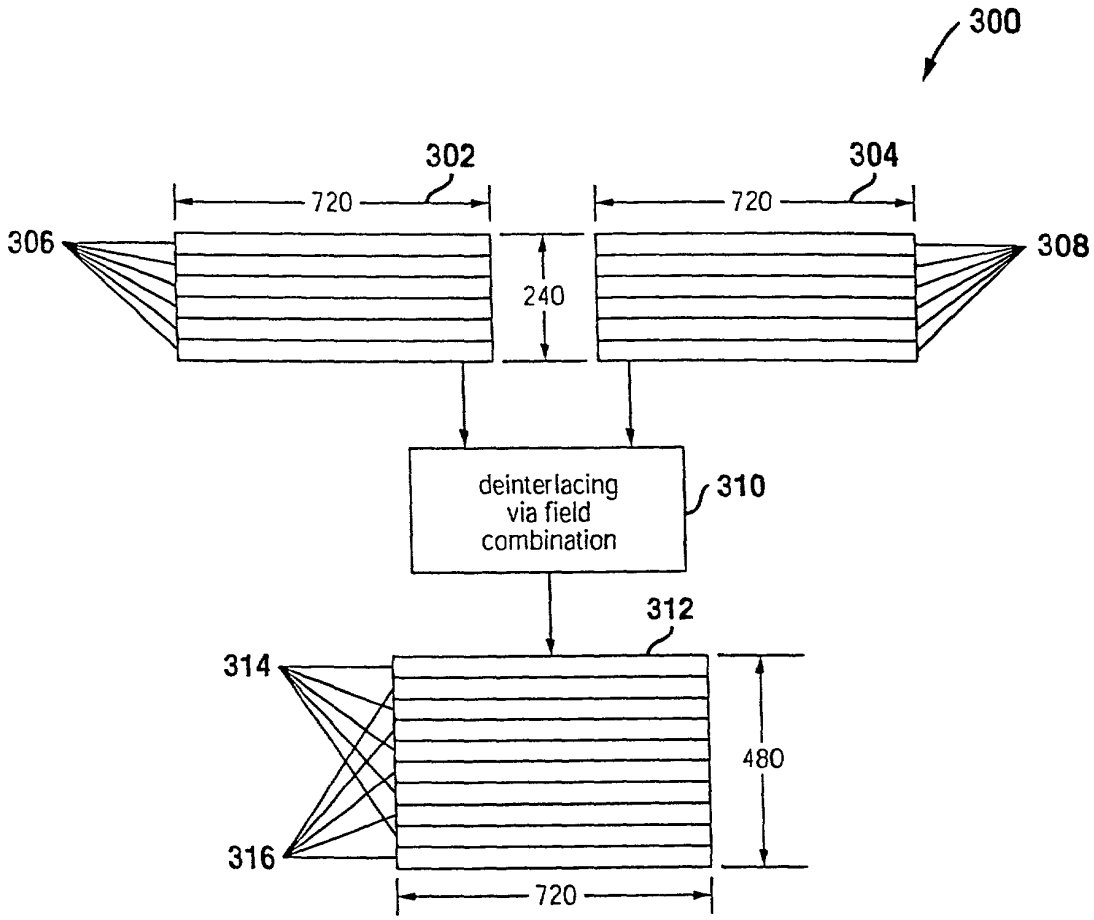
300
302
304
720
720
306
308
240
deinterlacing
via field
combination
310
312
314
480
316
720

Fig. 11

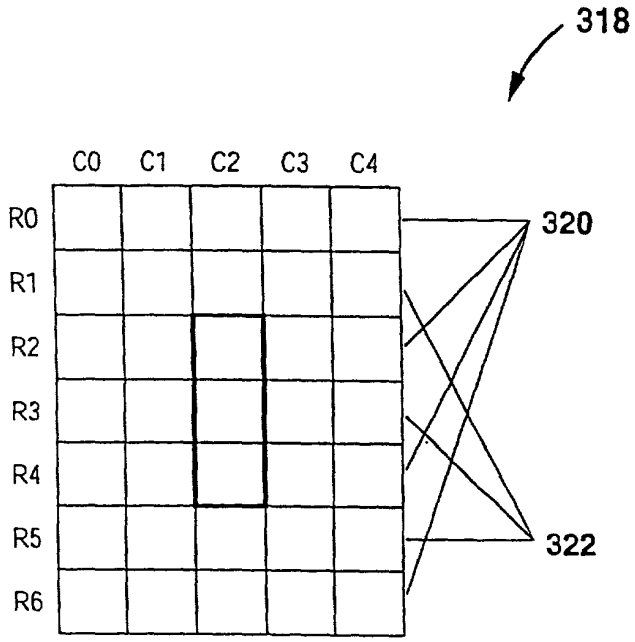

Fig. 12

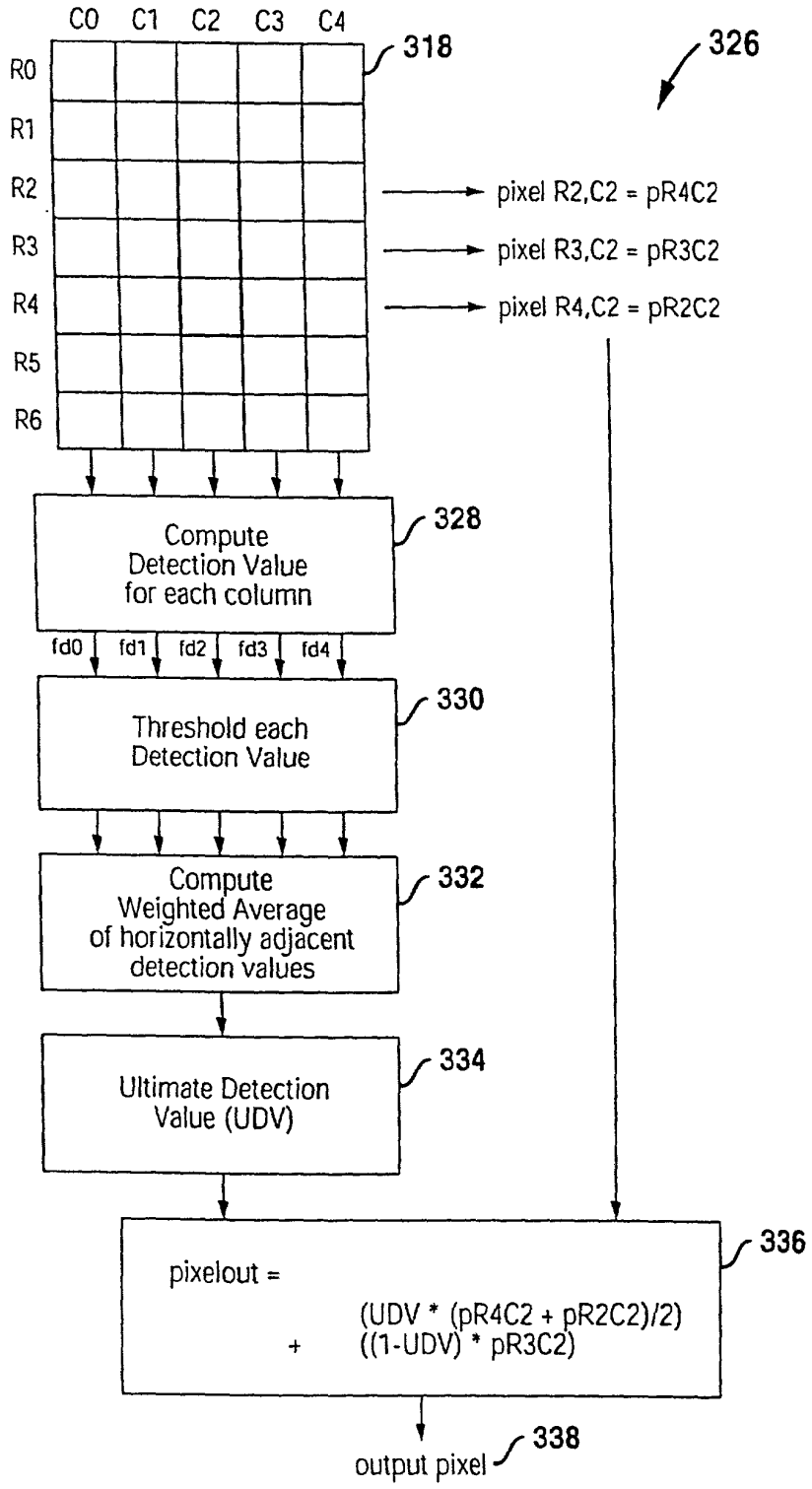
C0
C1
C2
C3
C4
R0
R1
R2
R3
R4
R5
R6
318
326
pixel R2,C2 = pR4C2
pixel R3,C2 = pR3C2
pixel R4,C2 = pR2C2
Compute Detection Value for each column
328
fd0
fd1
fd2
fd3
fd4
Threshold each Detection Value
330
Compute Weighted Average of horizontally adjacent detection values
332
Ultimate Detection Value (UDV)
334
pixelout =
(UDV * (pR4C2 + pR2C2)/2)
+ ((1-UDV) * pR3C2)
336
output pixel
338

Fig. 13

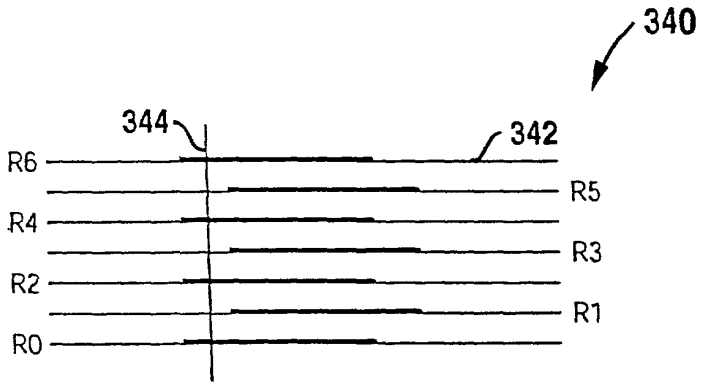

Fig. 14A

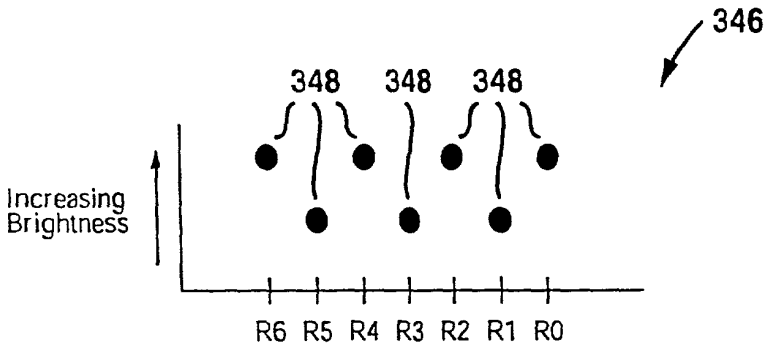

Fig. 14B

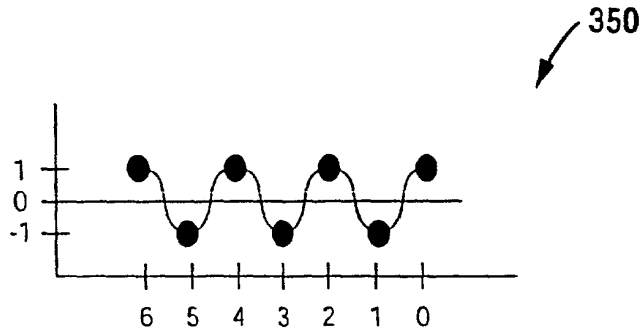

Fig. 14C

20030136 - 060402

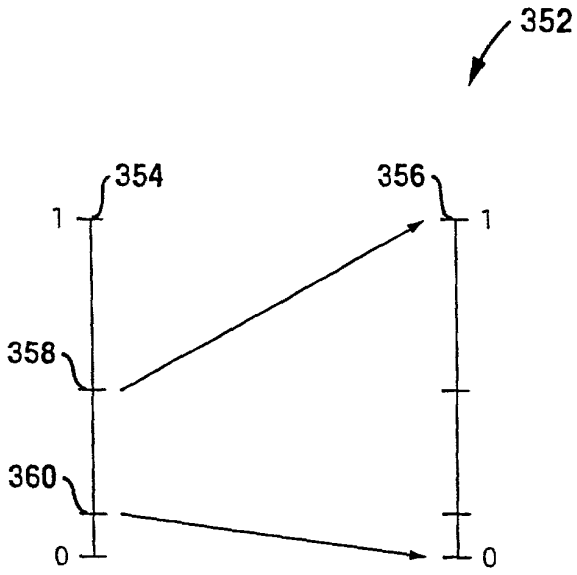

Fig. 15

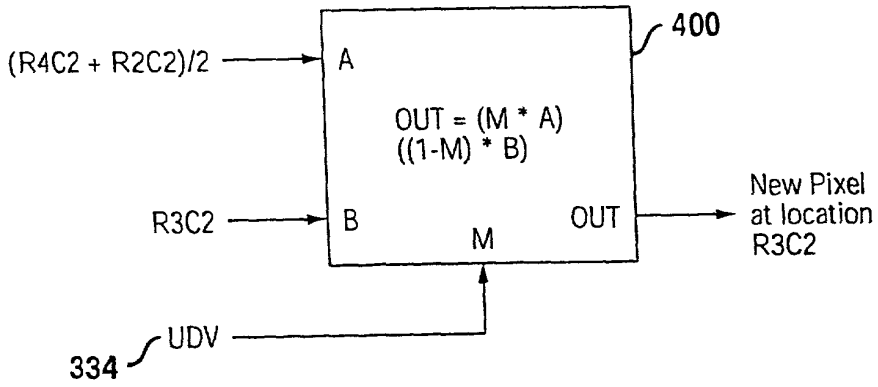
(R4C2 + R2C2)/2
A
400
OUT = (M * A)
((1-M) * B)
R3C2
B
M
OUT
New Pixel
at location
R3C2
334
UDV

Fig. 16

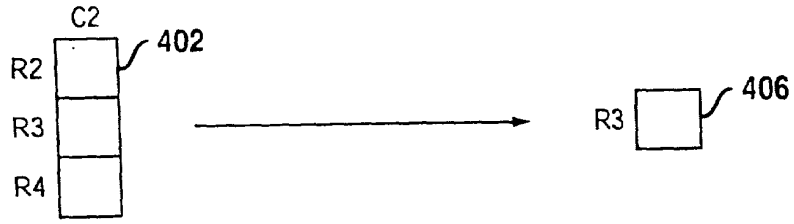
C2
R2
R3
R4
402
R3
406

Fig. 17

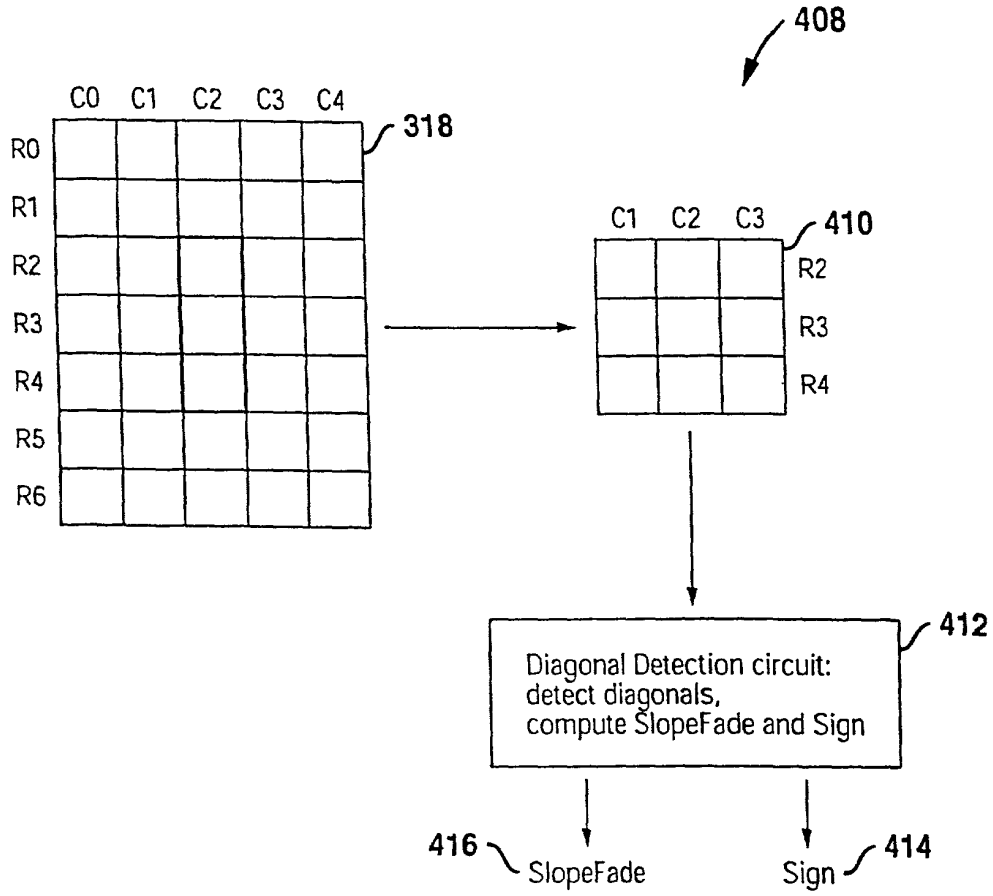
408
C0 C1 C2 C3 C4
318
R0
R1
R2
R3
R4
R5
R6
C1 C2 C3
410
R2
R3
R4
Diagonal Detection circuit:
detect diagonals,
compute SlopeFade and Sign
412
416
SlopeFade
Sign
414

Fig. 18

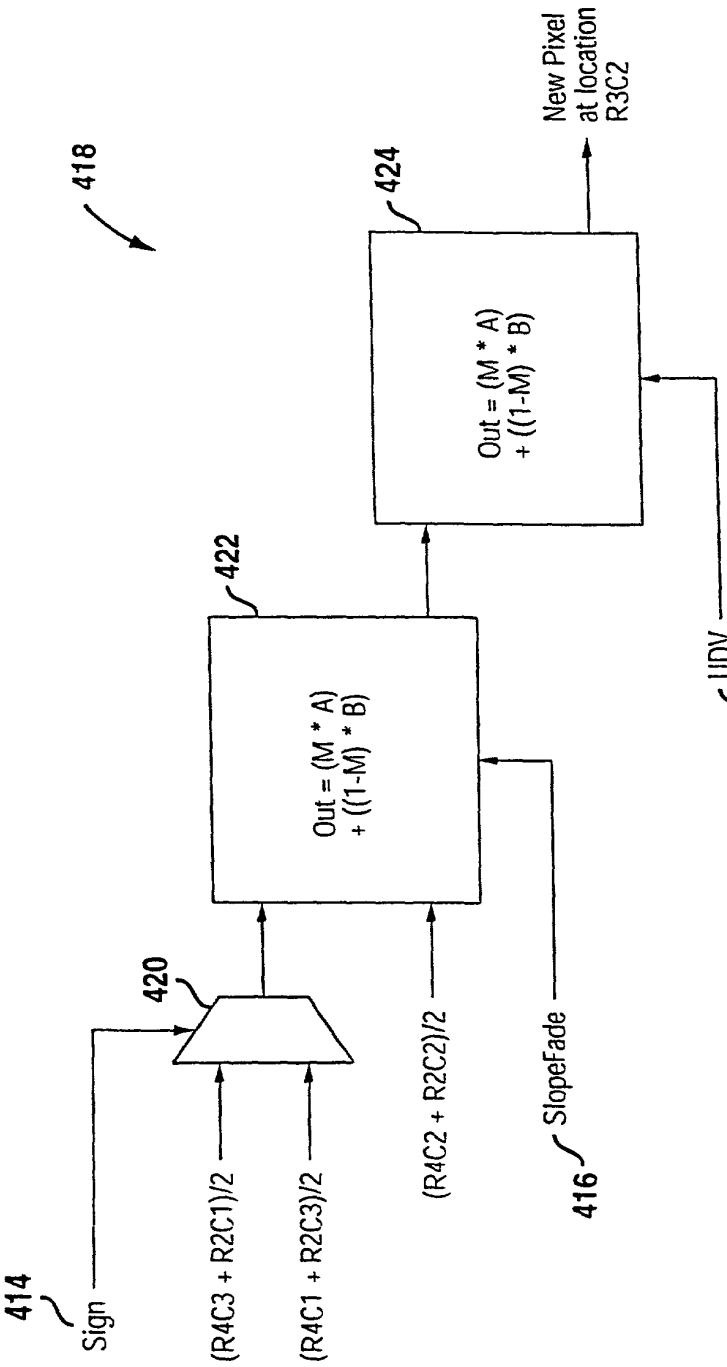
418
424
New Pixel at location R3C2
Out = (M * A) + ((1-M) * B)
422
Out = (M * A) + ((1-M) * B)
UDV
334
420
414
Sign
(R4C3 + R2C1)/2
(R4C1 + R2C3)/2
(R4C2 + R2C2)/2
SlopeFade
416

Fig. 19

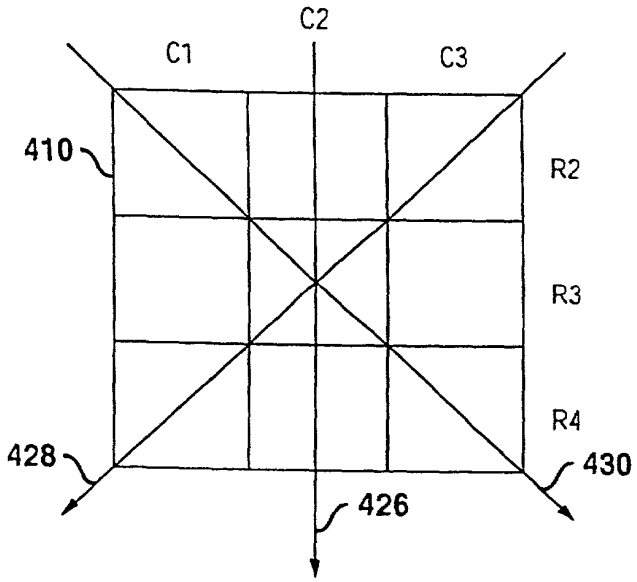

Fig. 20

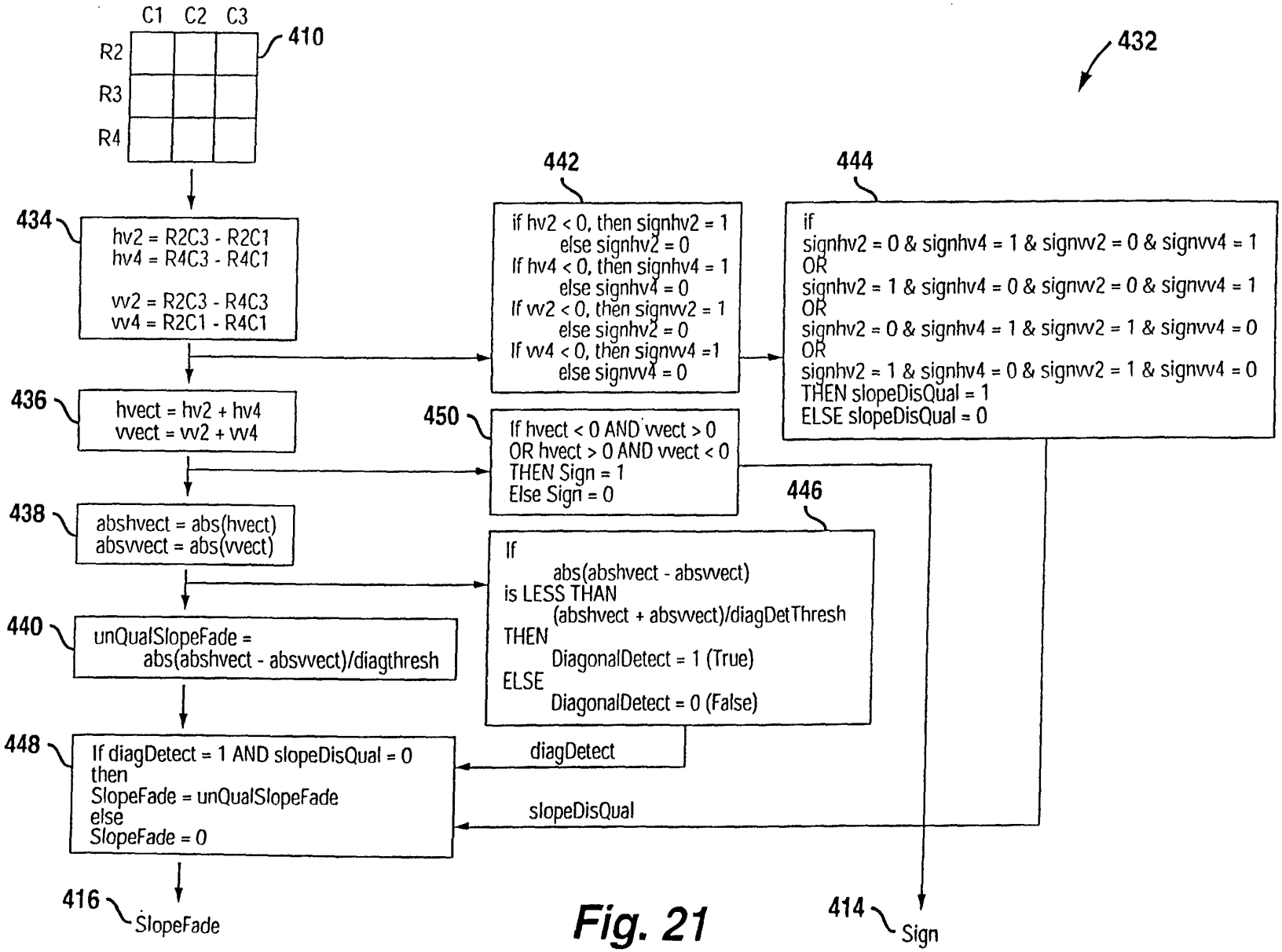

Fig. 21

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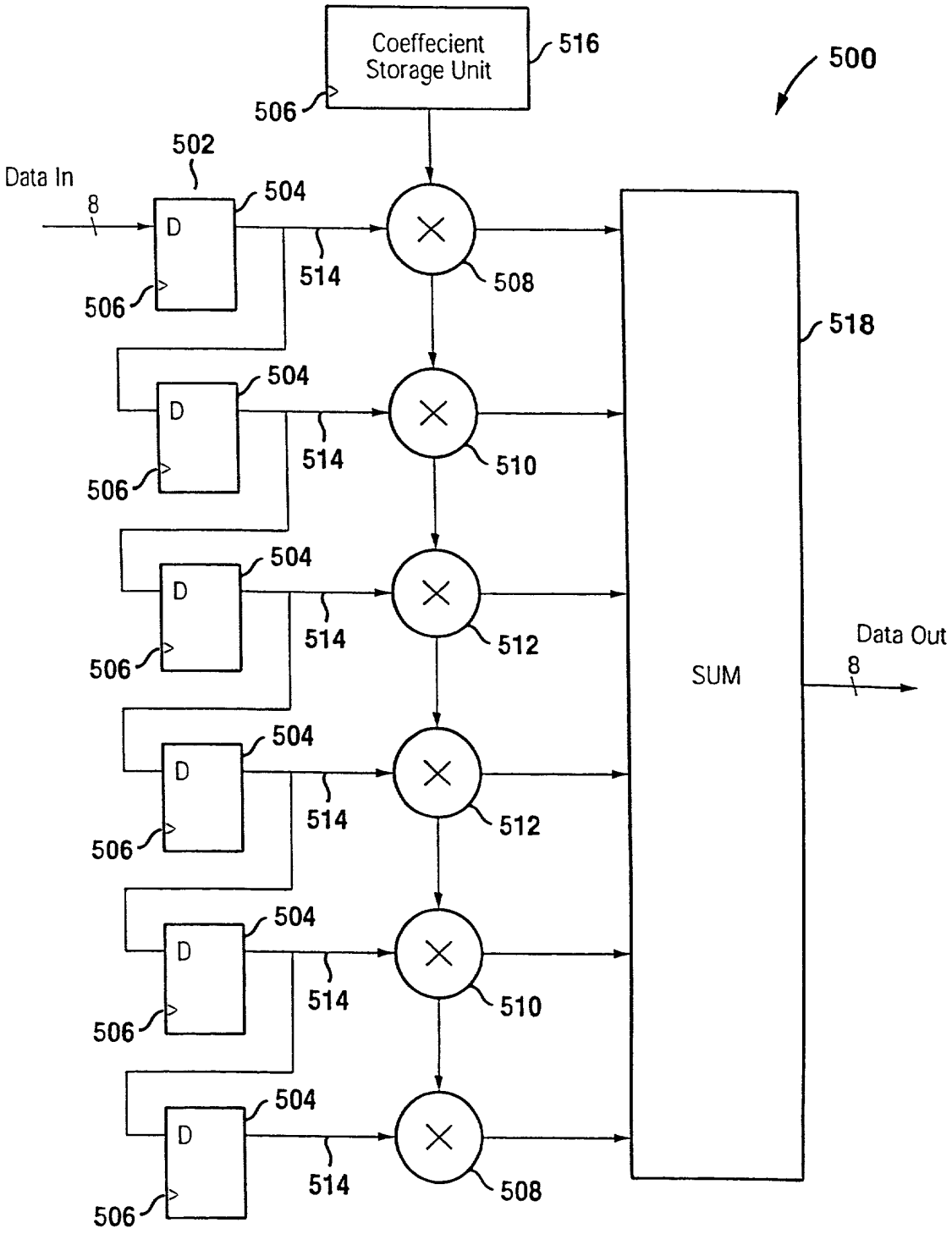

Coeffecient Storage Unit
516
500
506
502
Data In
8
504
D
514
508
518
510
512
SUM
Data Out
8

Fig. 22

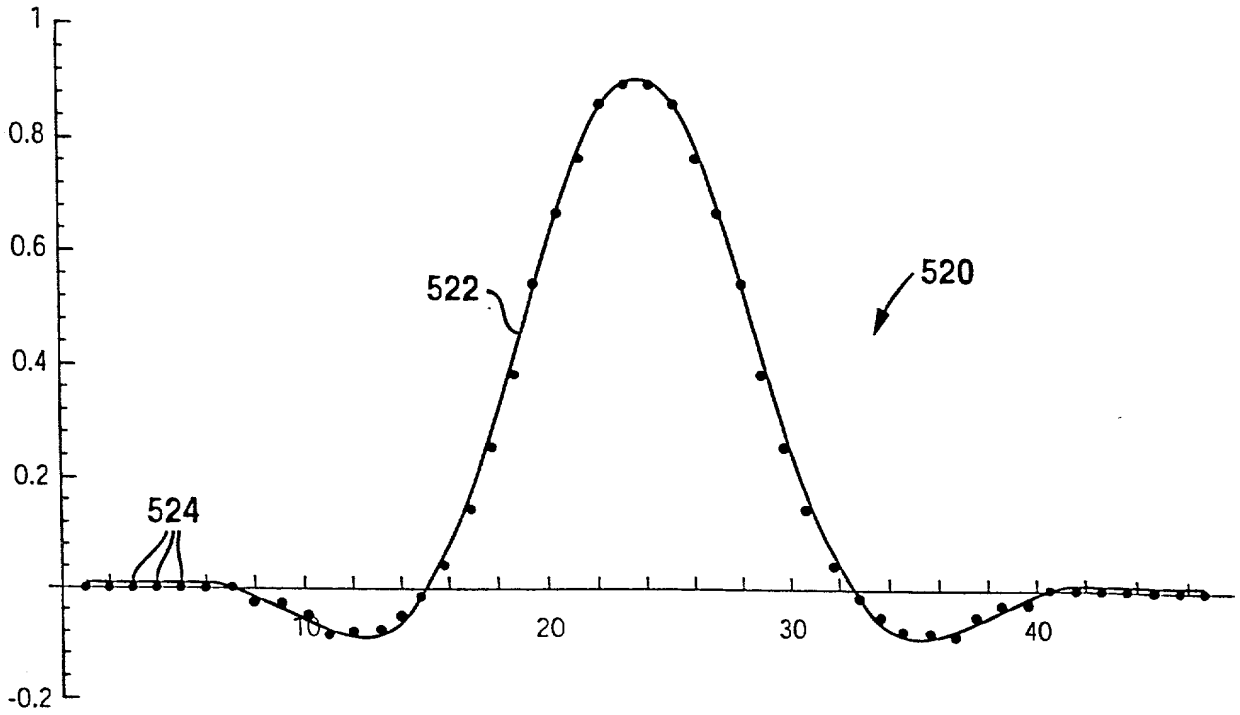


Fig. 23

set(1)	c(1), c(9), c(17), c(25), c(33), c(41)
set(2)	c(2), c(10), c(18), c(26), c(34), c(42)
set(3)	c(3), c(11), c(19), c(27), c(35), c(43)
set(4)	c(4), c(12), c(20), c(28), c(36), c(44)
set(5)	c(5), c(13), c(21), c(29), c(37), c(45)
set(6)	c(6), c(14), c(22), c(30), c(38), c(46)
set(7)	c(7), c(15), c(23), c(31), c(39), c(47)
set(8)	c(8), c(16), c(24), c(32), c(40), c(48)

Fig. 24

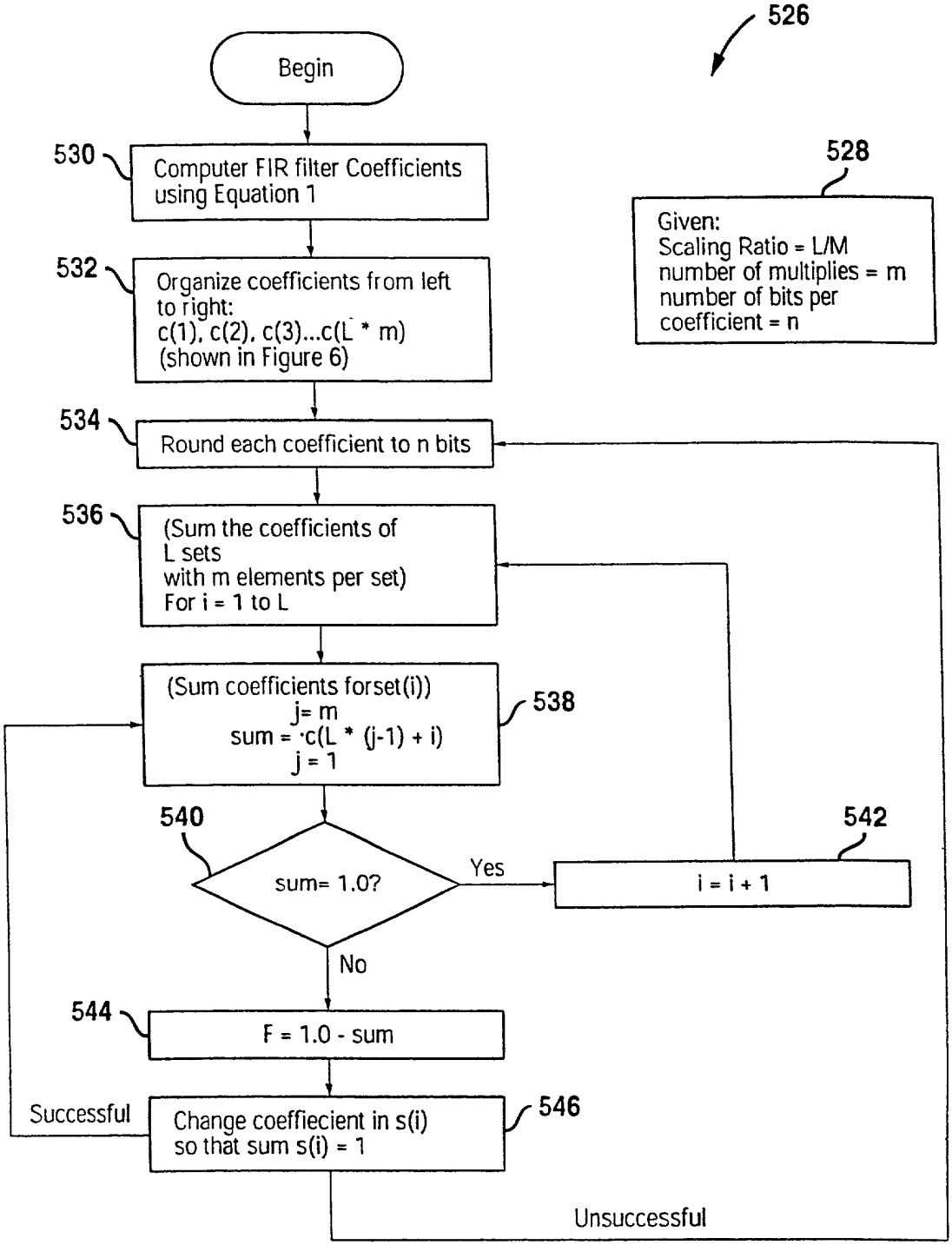

526
Begin
530
Computer FIR filter Coefficients using Equation 1
528
Given:
Scaling Ratio = L/M
number of multiplies = m
number of bits per coefficient = n
532
Organize coefficients from left to right:
c(1), c(2), c(3)...c(L * m)
(shown in Figure 6)
534
Round each coefficient to n bits
536
(Sum the coefficients of
L sets
with m elements per set)
For i = 1 to L
(Sum coefficients forset(i))
j= m
sum = c(L * (j-1) + i)
j = 1
538
540
sum= 1.0?
Yes
542
i = i + 1
No
544
F = 1.0 - sum
Successful
Change coeffiecient in s(i)
so that sum s(i) = 1
546
Unsuccessful

Fig. 25

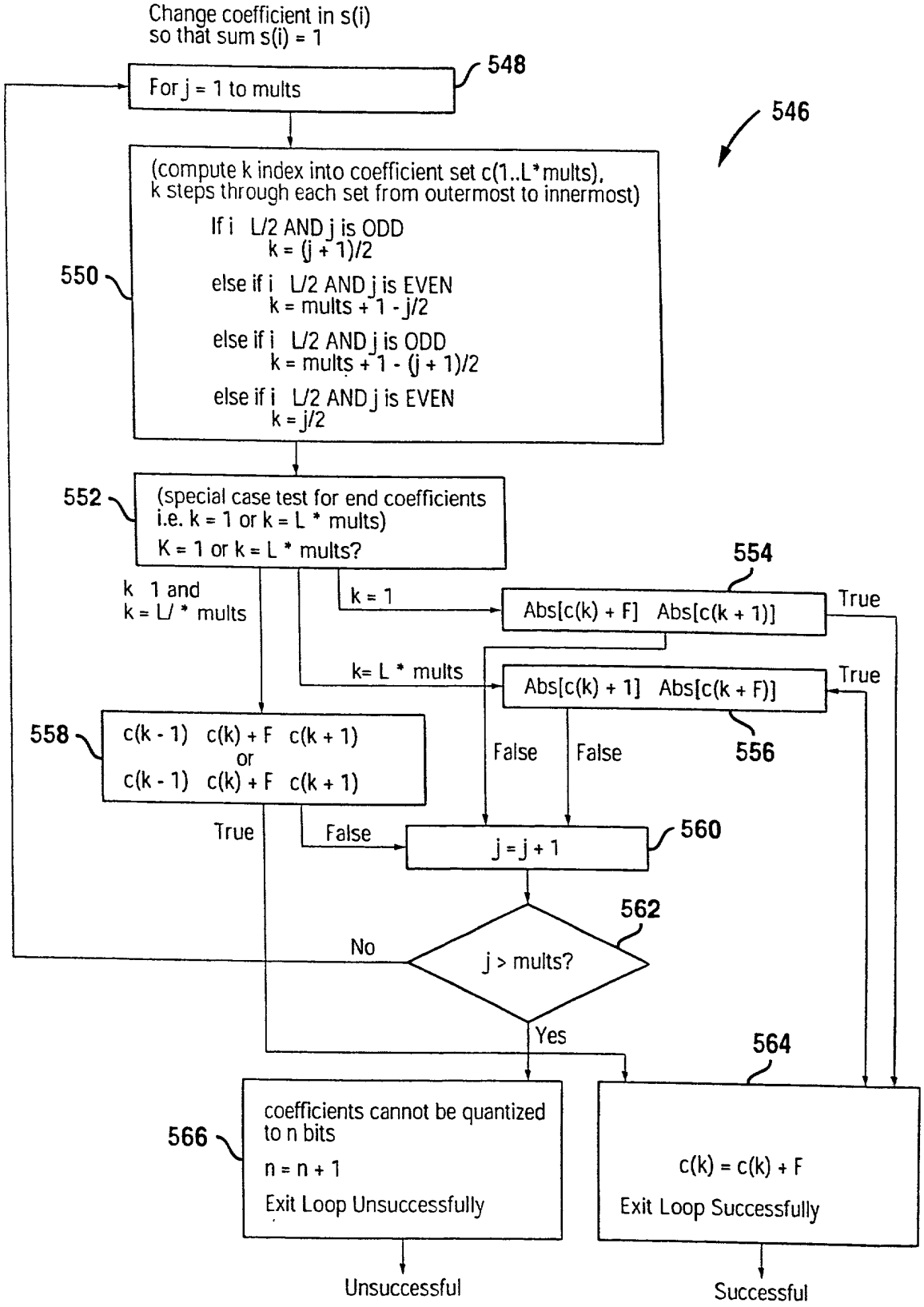

Change coefficient in s(i)
so that sum s(i) = 1
For j = 1 to mults
548
546
(compute k index into coefficient set c(1..L*mults),
k steps through each set from outermost to innermost)
If i L/2 AND j is ODD
k = (j + 1)/2
else if i L/2 AND j is EVEN
k = mults + 1 - j/2
else if i L/2 AND j is ODD
k = mults + 1 - (j + 1)/2
else if i L/2 AND j is EVEN
k = j/2
550
(special case test for end coefficients
i.e. k = 1 or k = L * mults)
K = 1 or k = L * mults?
552
k 1 and
k = L/ * mults
k = 1
k= L * mults
554
Abs[c(k) + F] Abs[c(k + 1)]
True
Abs[c(k) + 1] Abs[c(k + F)]
True
556
False
False
558
c(k - 1) c(k) + F c(k + 1)
or
c(k - 1) c(k) + F c(k + 1)
True
False
j = j + 1
560
562
No
j > mults?
Yes
564
566
coefficients cannot be quantized
to n bits
n = n + 1
Exit Loop Unsuccessfully
c(k) = c(k) + F
Exit Loop Successfully
Unsuccessful
Successful

Fig. 26

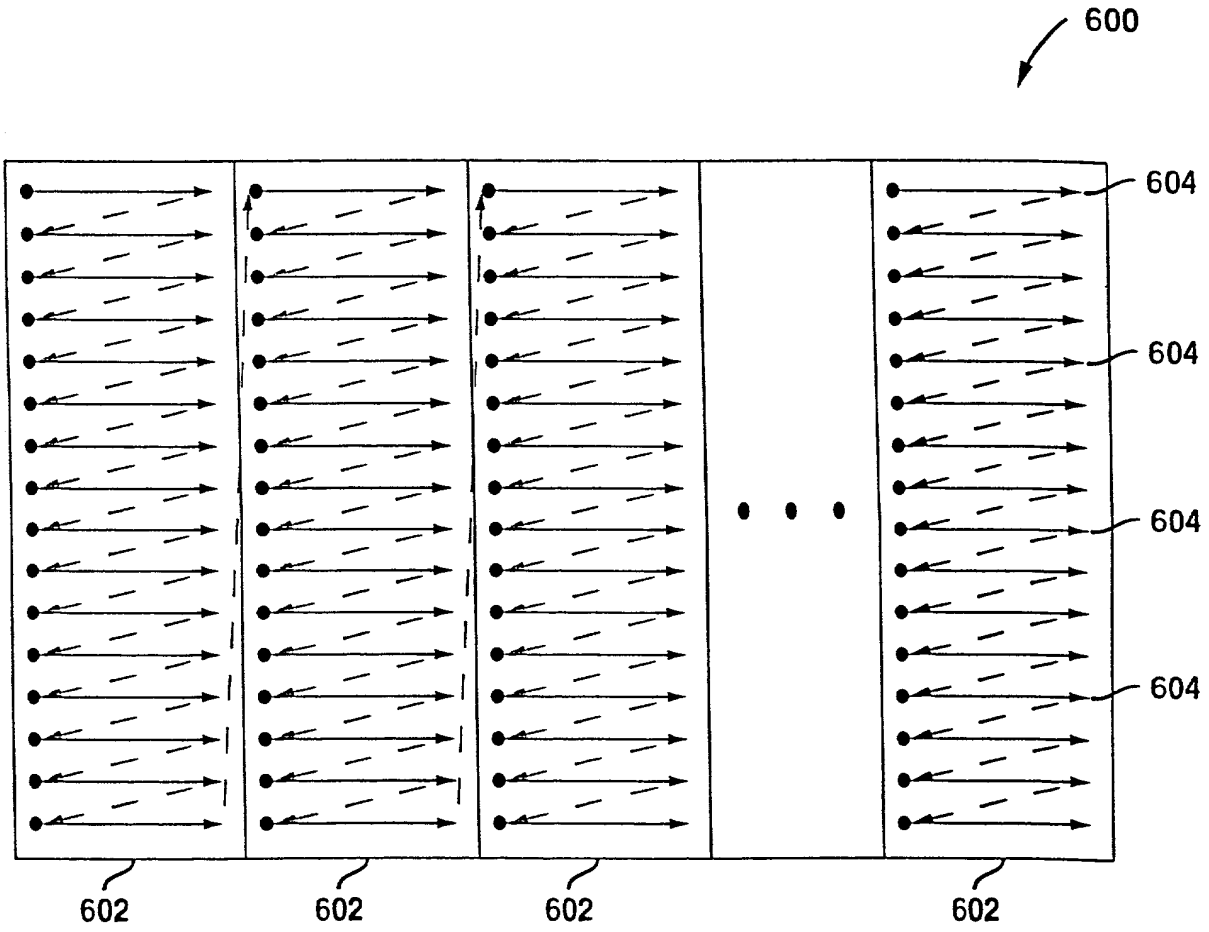


Fig. 27

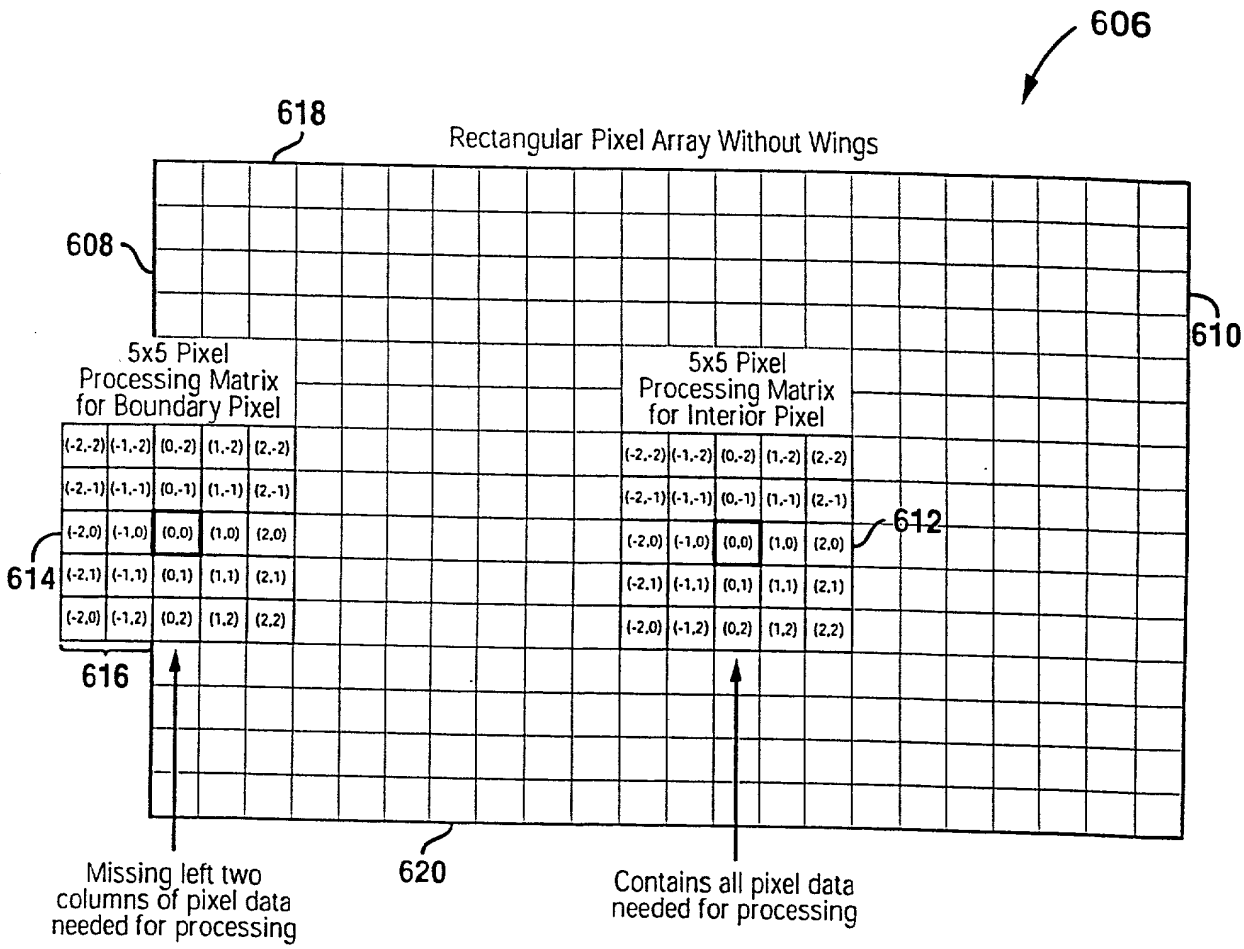

606
618
Rectangular Pixel Array Without Wings
608
610
5x5 Pixel Processing Matrix for Boundary Pixel
5x5 Pixel Processing Matrix for Interior Pixel
612
614
616
620
Missing left two columns of pixel data needed for processing
Contains all pixel data needed for processing

Fig. 28

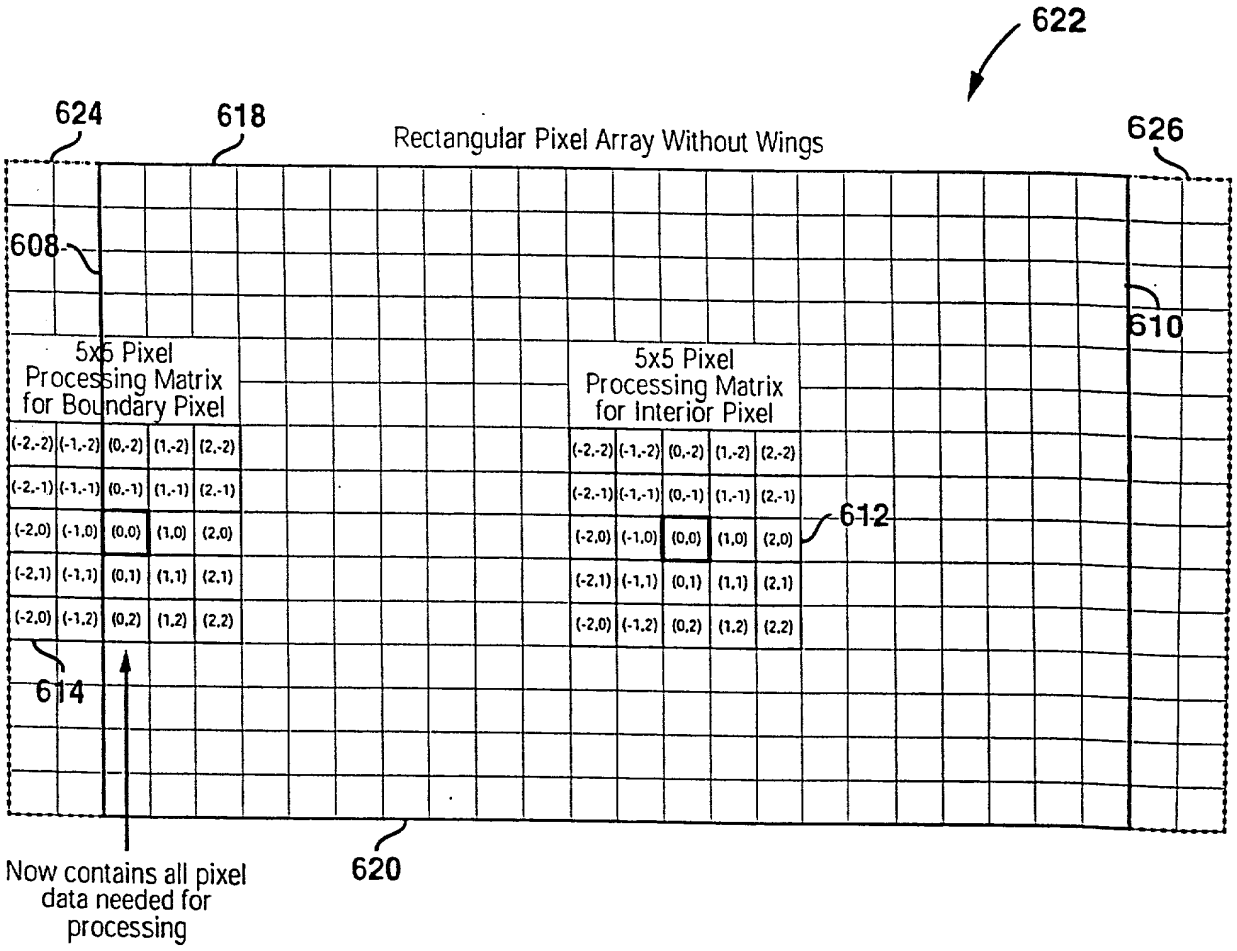

622
624
618
Rectangular Pixel Array Without Wings
626
608
610
5x5 Pixel Processing Matrix for Boundary Pixel
5x5 Pixel Processing Matrix for Interior Pixel
612
614
620
Now contains all pixel data needed for processing

Fig. 29

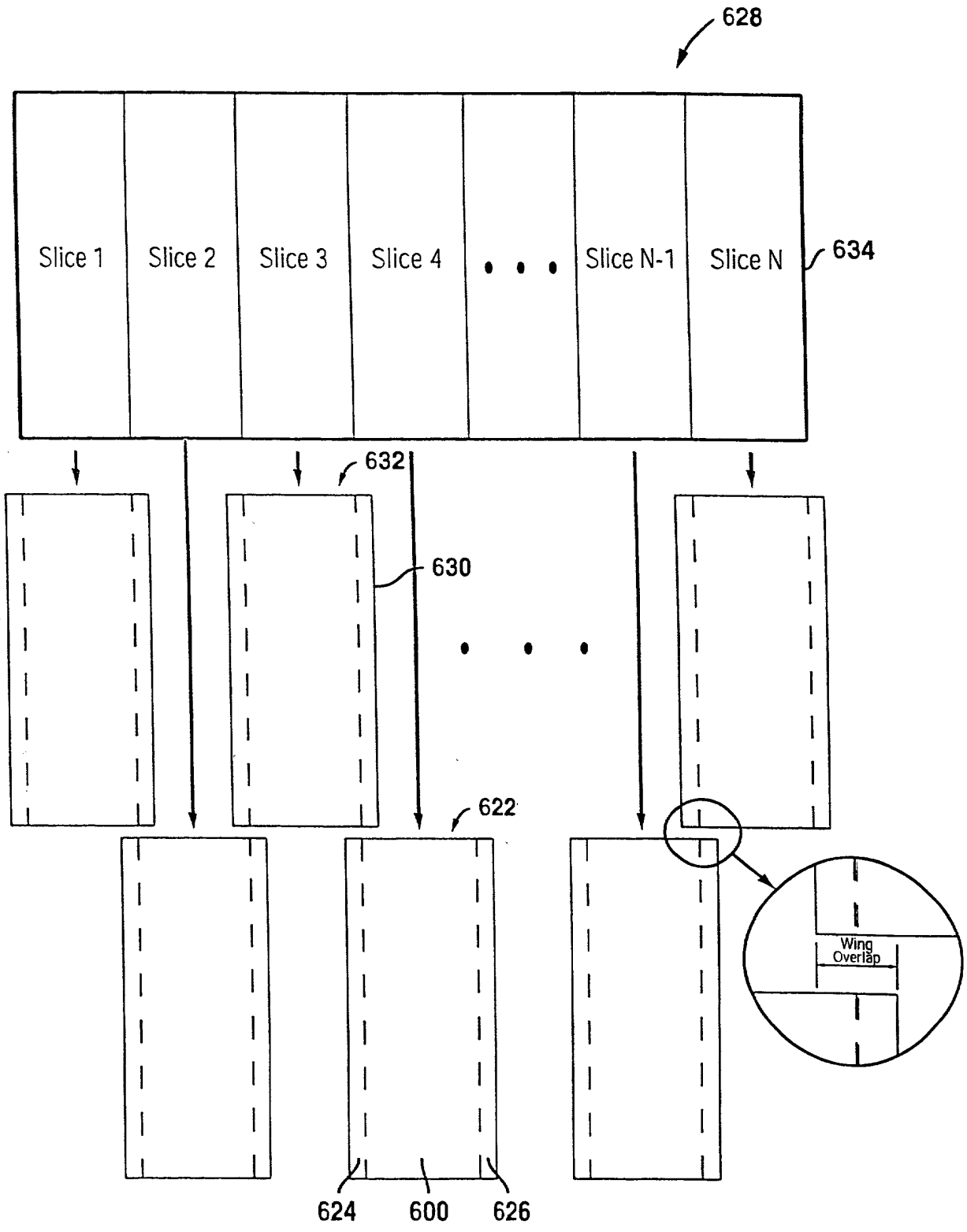

628
Slice 1
Slice 2
Slice 3
Slice 4
Slice N-1
Slice N
634
632
630
622
Wing Overlap
624
600
626

Fig. 30

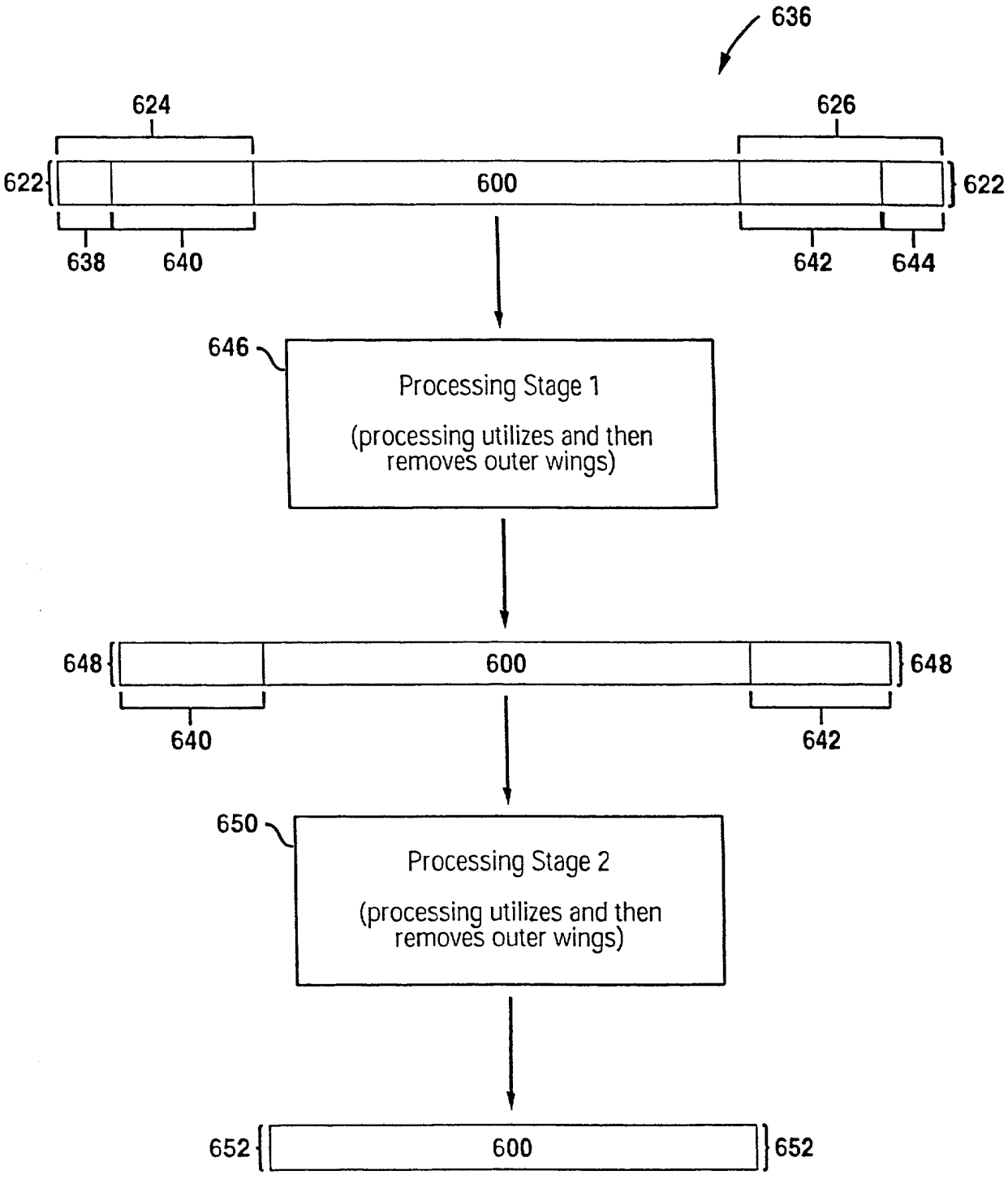


Fig. 31

Attorney Docket No. 60472-301302

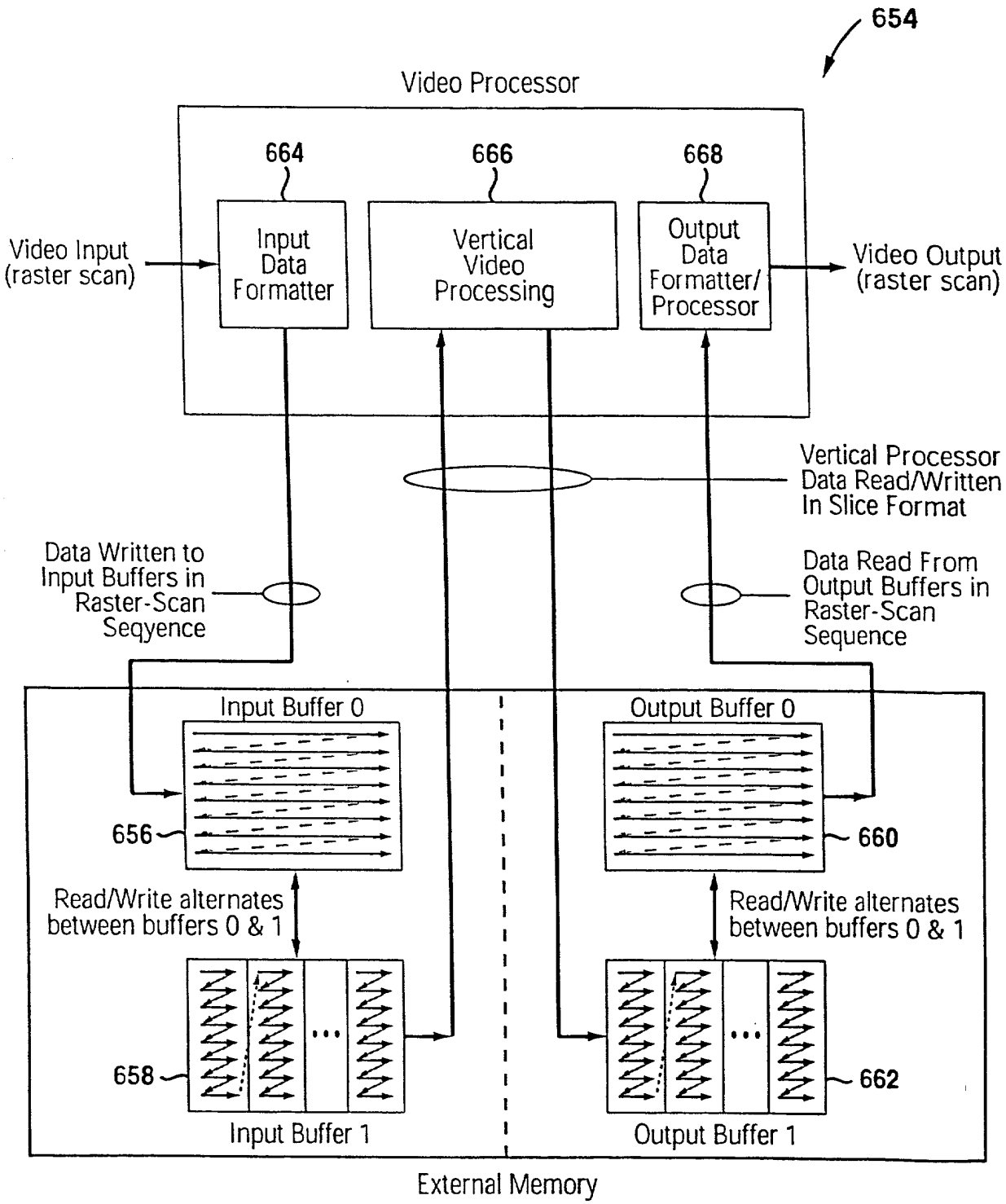

654
Video Processor
664
666
668
Input Data Formatter
Vertical Video Processing
Output Data Formatter/ Processor
Video Input (raster scan)
Video Output (raster scan)
Vertical Processor Data Read/Written In Slice Format
Data Written to Input Buffers in Raster-Scan Seqyence
Data Read From Output Buffers in Raster-Scan Sequence
Input Buffer 0
Output Buffer 0
656
660
Read/Write alternates between buffers 0 & 1
Read/Write alternates between buffers 0 & 1
658
662
Input Buffer 1
Output Buffer 1
External Memory

Fig. 32

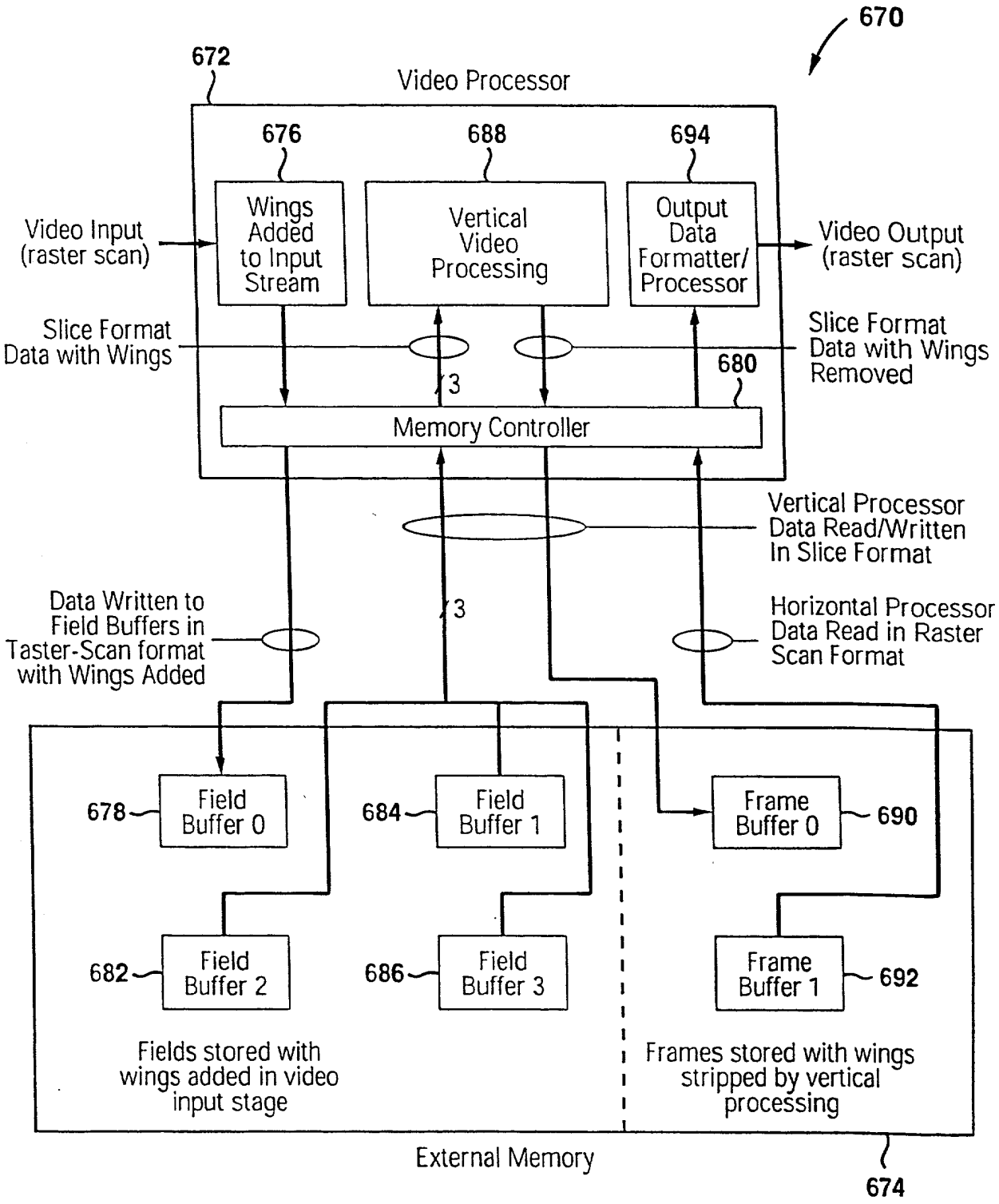

670
672
Video Processor
676
688
694
Wings Added to Input Stream
Vertical Video Processing
Output Data Formatter/ Processor
Video Input (raster scan)
Video Output (raster scan)
Slice Format Data with Wings
Slice Format Data with Wings Removed
680
3
Memory Controller
Vertical Processor Data Read/Written In Slice Format
Data Written to Field Buffers in Taster-Scan format with Wings Added
3
Horizontal Processor Data Read in Raster Scan Format
678
Field Buffer 0
684
Field Buffer 1
Frame Buffer 0
690
682
Field Buffer 2
686
Field Buffer 3
Frame Buffer 1
692
Fields stored with wings added in video input stage
Frames stored with wings stripped by vertical processing
External Memory
674

Fig. 33

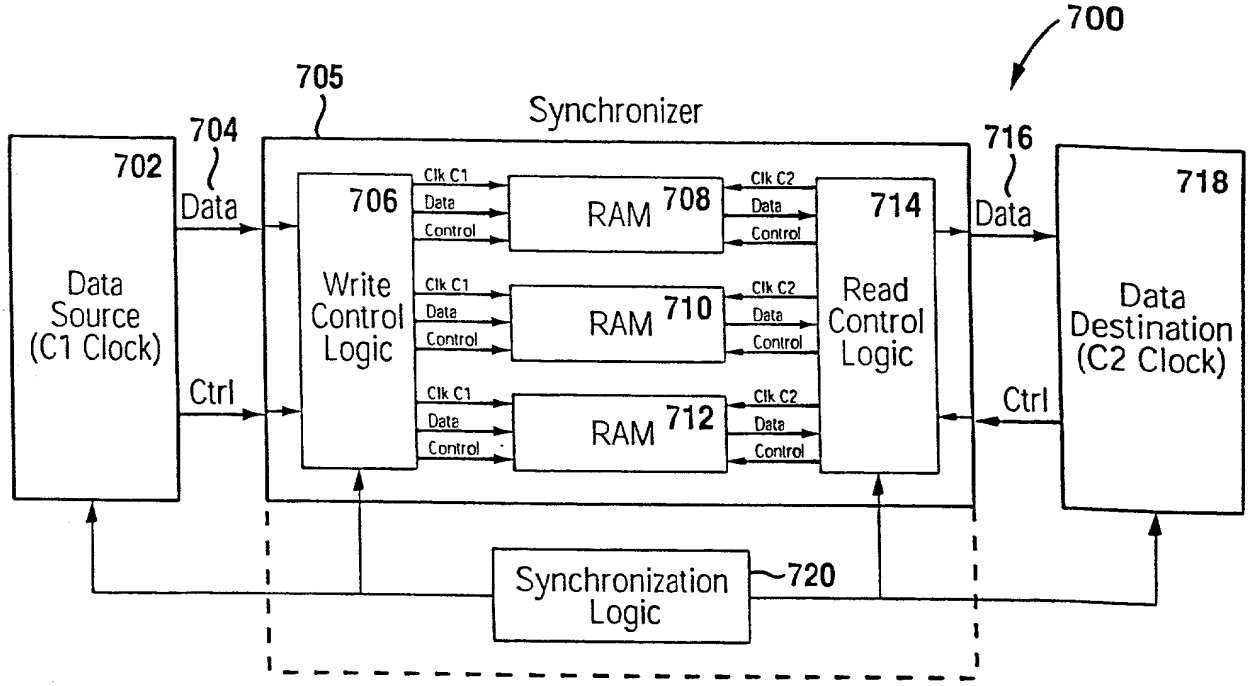

700
705
Synchronizer
704
Data
Ctrl
702
Data Source (C1 Clock)
706
Write Control Logic
Clk C1
Data
Control
RAM 708
RAM 710
RAM 712
Clk C2
714
Read Control Logic
716
Data
Ctrl
718
Data Destination (C2 Clock)
Synchronization Logic
720

Fig. 34

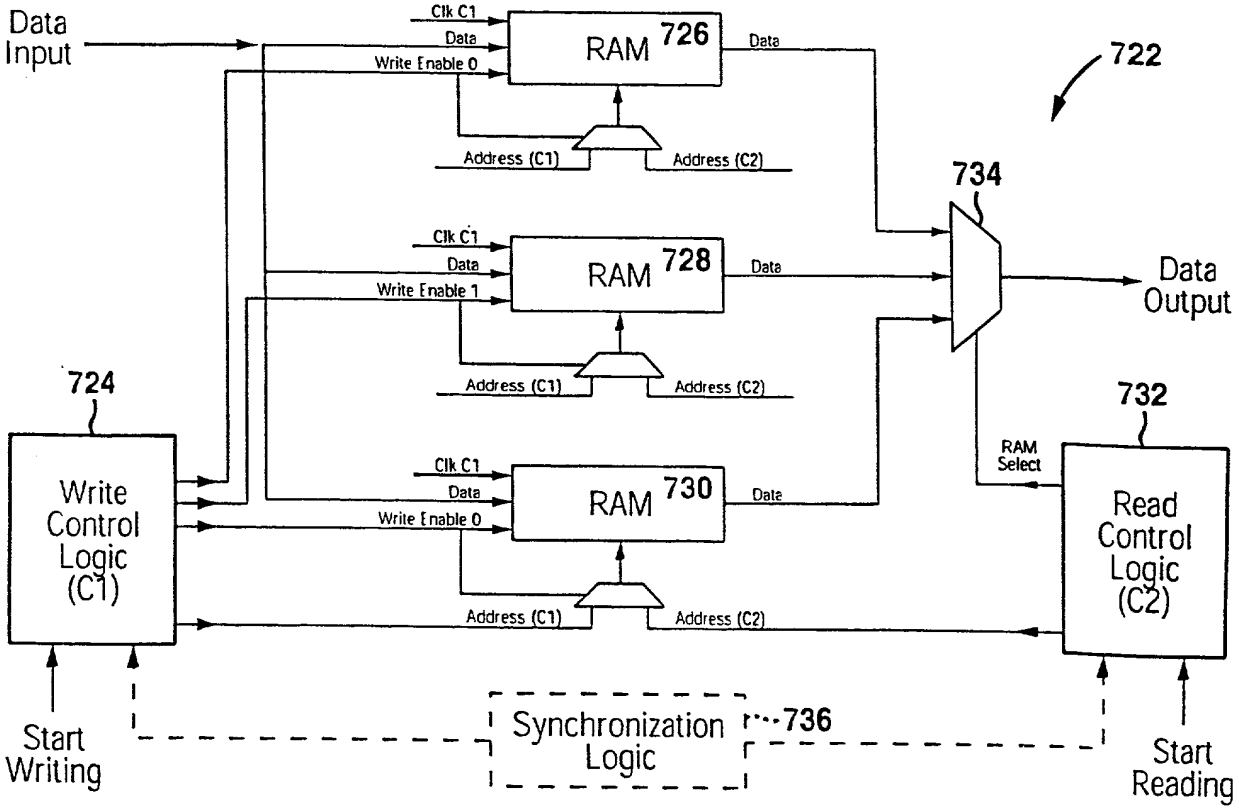
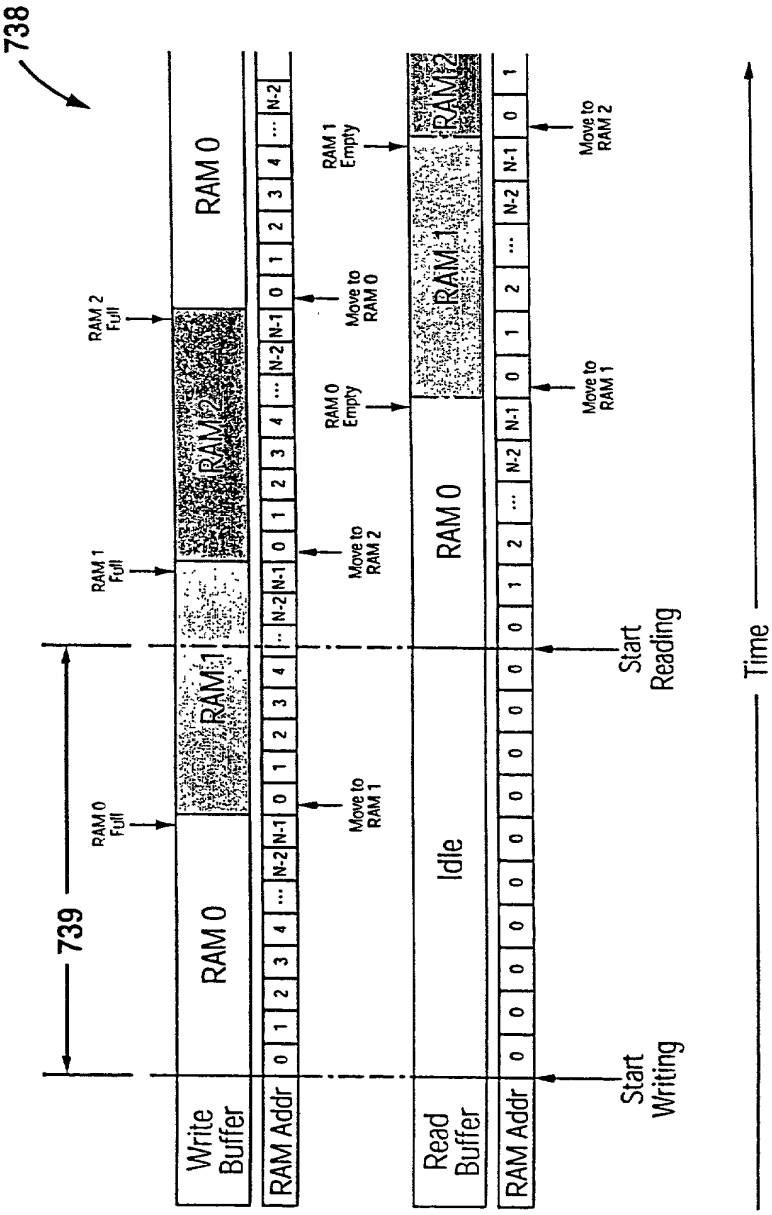
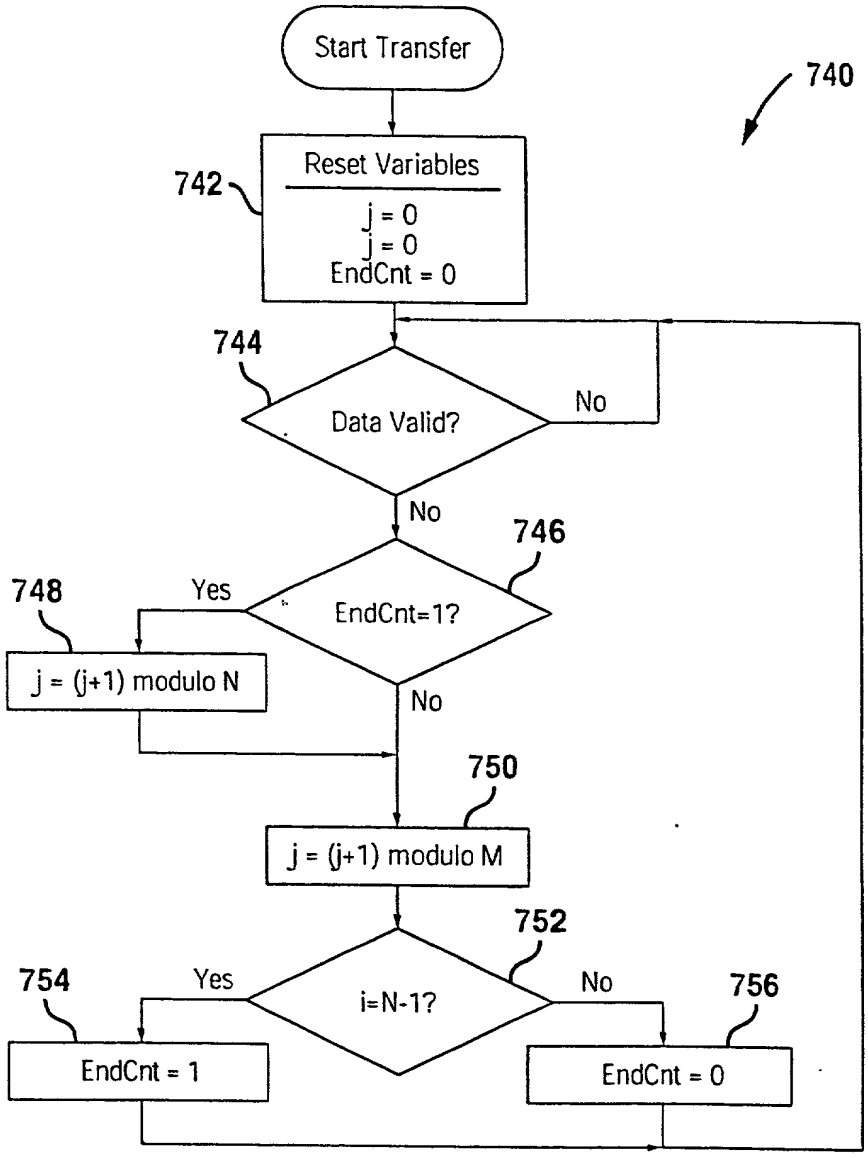

Data Input
Clk C1
Data
Write Enable 0
RAM 726
Data
722
Address (C1)
Address (C2)
734
Clk C1
Data
Write Enable 1
RAM 728
Data
Data Output
724
Write Control Logic (C1)
Clk C1
Data
Write Enable 0
RAM 730
Data
732
RAM Select
Read Control Logic (C2)
Address (C1)
Address (C2)
Start Writing
Synchronization Logic
736
Start Reading

Fig. 35



NOTE: Each RAM has n addressable locations.

Fig. 36



NOTES:
1. "i" is the RAM Address.
2. "j" denotes the selected RAM module the address MUX control and RAM write enable.
3. "EndCnt" indicates that the RAM Address points to the last location in a RAM module.
4. "M" is the number of addressable location in a RAM module.
5. "N" is the number of RAM modules.

Fig. 37

Replaced by new sheet

20f7+0" 9ET2E00T

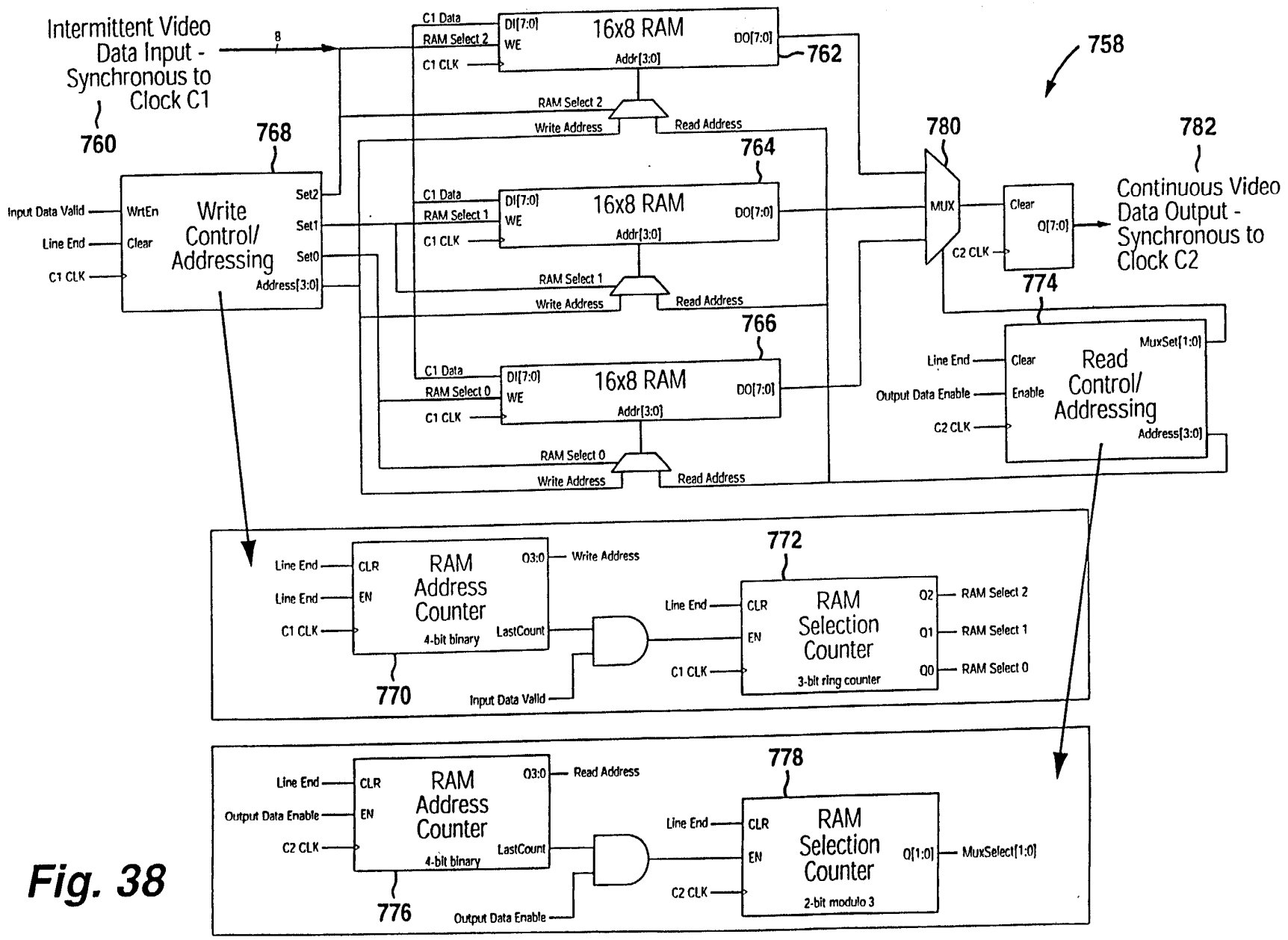


Fig. 38

OPPENHEIMER WOLFF & DONNELLY, LLP
Title: DIGITAL VIDEO SYSTEM AND METYHODS FOR PROVIDING SAME
U.S. Patent Application No. 10/032,136
Atty. Docket No.: 60472-301302
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